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TriBoard TC1796

Hardware Manual TC1796.300

Microcontrollers

Infineon technologies

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TriBoard TC1796 Hardware Manual TC1796.100

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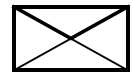

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1 Introduction

We congratulate you on your purchase of the TriCore Evaluation Board. This kit is a versatile tool, providing quick access to the capabilities of TriCore's powerful architecture.

Applications can be developed easily. The Evaluation Board is equipped with a variety of memories and peripherals for connection to the environment. There is also an interface for the On Chip Debugging Features (OCDS1 and OCDS2). The kit also includes several sets of development tools, which are stored on the included Evaluation Board CD-ROM.

The Evaluation Board allows easily the development of TriCore applications with the corresponding tools.

Subsequently, the applications can be downloaded and can be tested with the powerful debugger software.

This TriBoard Hardware Manual familiarizes you with the TriCore Evaluation Board and guides you through the initial setup of the TriBoard and the installation of the development software tool chain.

2 TriBoard Features

- CPU: - TC1796 (TriCore)
- MEMORY: - Burst FLASH up to 16 MBytes (default:4 MBytes)
  - asynchronous SRAM up to 1MBytes (default)
  - optional synchronous SRAM up to 8 MBytes
- CLOCK: - Crystal 20MHz (default), Oscillator or External Clock
- INTERFACE: - DB9 for RS232-0
  - BERG10 for RS232-1
  - two BERG10 for CAN-0/1 with Transceiver
  - BERG16 for OCDS1
  - SAMTEC QSH-030-01-F-D-A for OCDS2
  - DB25 On Board Wiggler for OCDS1
  - four 80-pin connectors (male) with all I/O signals
  - four 80-pin connectors (female) with all I/O signals
- POWER: - 5,5V to 60V
  - generated internally 3.3V, 1.5V (optional 2.5V for Bussystem)
  - generated internally 5V for OnBoard Wiggler and CAN Transceiver
  - Power On Reset circuit
- DIMENSION: - 100mm x 160mm (EURO-Board)

2.1 Block Diagram

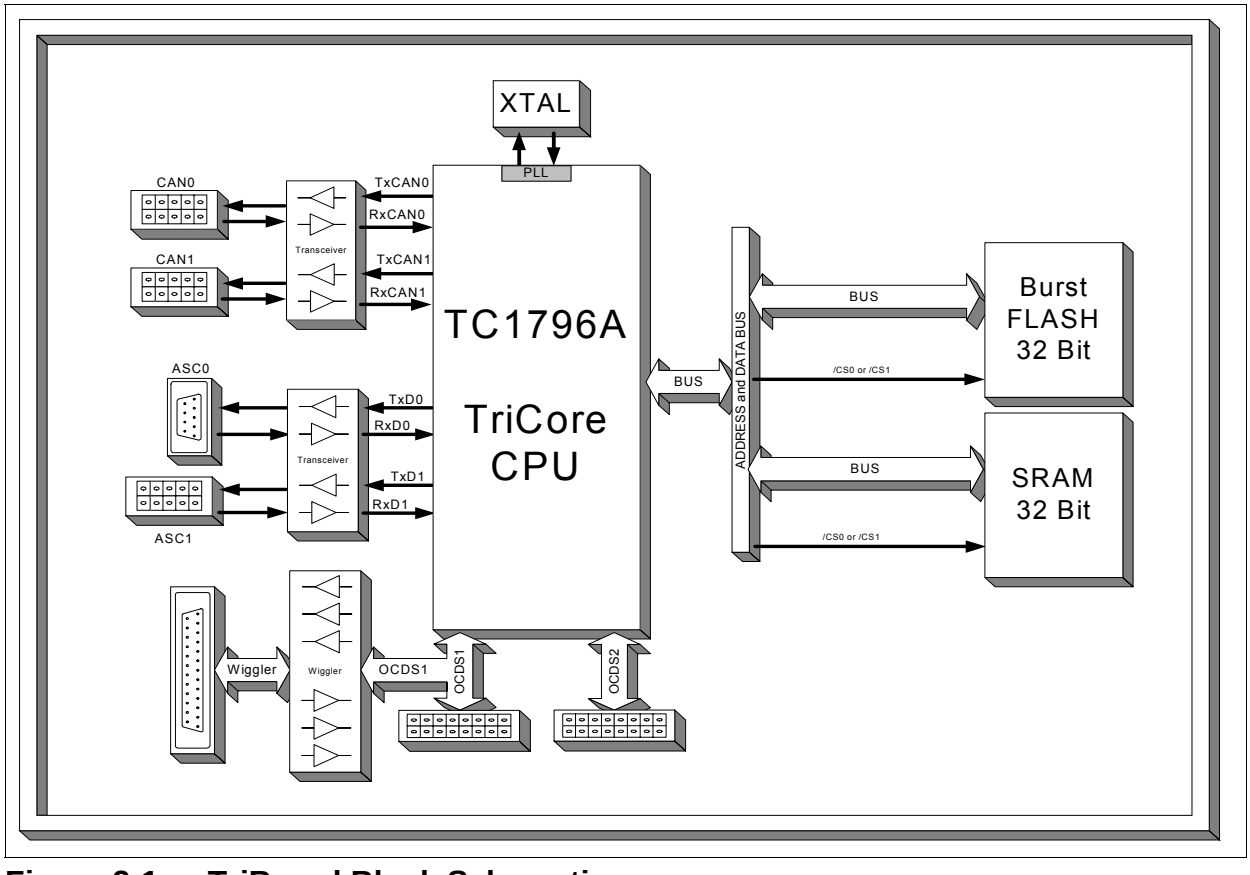

Figure 2-1 TriBoard Block Schematic

2.2 Placement

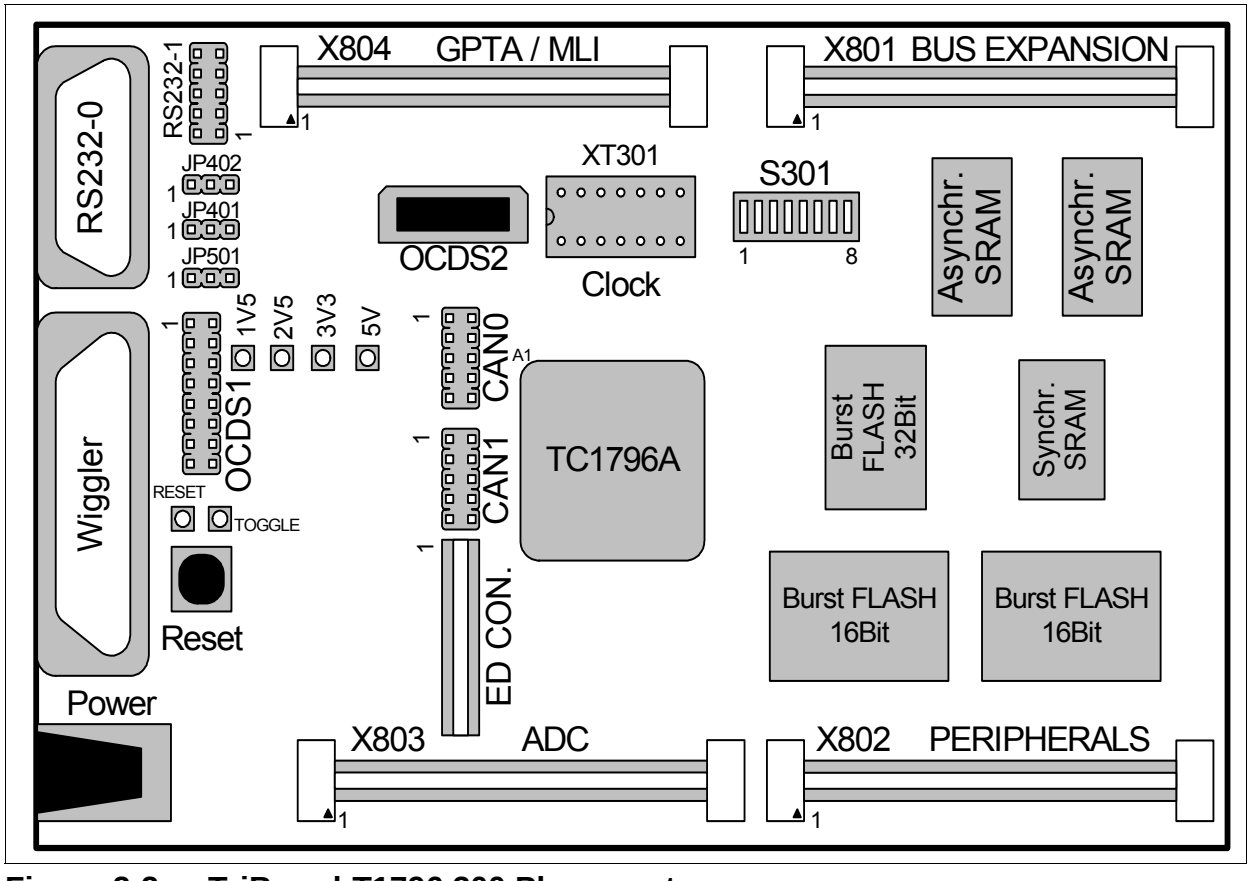

Figure 2-2 TriBoard-T1796.300 Placement

3 Getting Started

This section provides a basic understanding of how to upload a program to the TriBoard and run the debugger. In this example the software from Tasking Version 1.5r1 or higher will be used to explain the first steps. The needed driver for debugging runs only with WindowsNT 4.00 and Windows 2000. To install the driver you need “Power User” or “Administrator” rights, because editing of the registry is required.

3.1 Install the Tasking EDE Software.

A demo of the Tasking Software can be found in the WWW under the URL:

http://www.tasking.com

Insert your Tasking CD on your CD drive and start “Setup.exe”, if the program is not executed automatic then change to your CD drive and start “Setup.exe” manually or download a demo from the Tasking website and start “Setup.exe” and follow the instructions.

3.2 Install the Driver for Debugging.

The Driver is located in the “\Tools\Driver\” directory. Start “Reg_JTAGdrv.exe”. Now copy all subdirectories from “\Tools\Driver\Tasking\” to your Tasking folder. The default location of the Tasking files is “C:\CTri\”. All files with the same name should be overwritten.

The file “ReadMe.txt” in this directory contains some additional informations. The driver works with only with Windows NT4.00 and Windows 2000.

3.3 Starting a New Tasking EDE >Project.

This section will be filled at the next release of TriBoard Manual for TC1796.

4 TriBoard Information

4.1 Power Supply

The Board has to be connected to a 5,5V to 60V DC power supply. The TriBoard generates internally 3.3V, 1.5V (optional 2.5V for the bussystem) and 5V. The power consumption is not specified yet but a supply with 7V and 500mA should be sufficient. The pinout for the supply connector is shown in **Figure 8-5**. There can be used any standard power pack with a connector where the positive line is surrounded by the ground line.

Applying a stable supply voltage causes the power on reset after a short period. The four LED's (5V, 3.3V, 2.5V, 1.5V) indicate the status of the on board generated voltage (if the LEDs are assembled).

A manual reset is executed by pressing the reset button.

4.2 Clock

There are three possibilities to apply the CPU clock.

- Large oscillator circuit (DIP14)
- Small oscillator circuit (DIP8)
- Crystal oscillator (default)
- External clock generator

The crystal oscillator and the oscillator circuit use the socket XT301. It's possible to apply a 14pol DIP oscillator package or an 8pol DIP oscillator package.

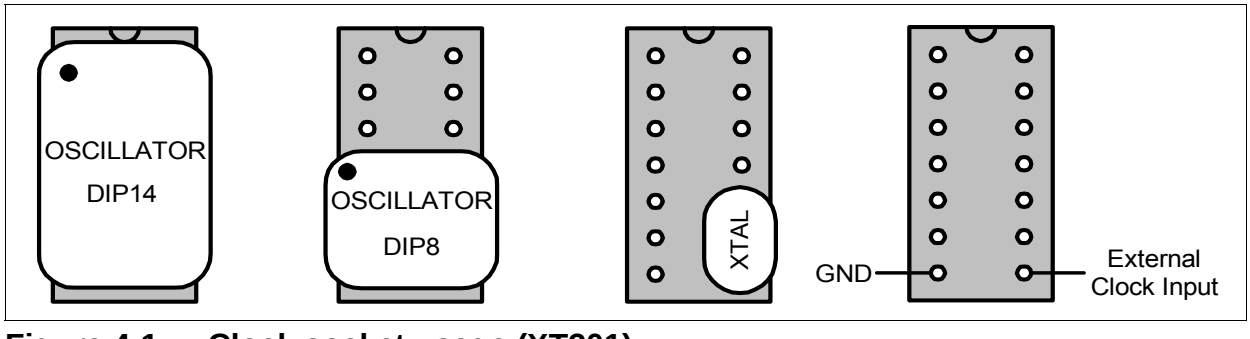

Figure 4-1 Clock socket usage (XT301)

4.3 Memory

The TriBoard supports the following memory configurations:

- up to 8 MBytes external Burst Flash (2x16Bit) or
- 4 MBytes external Burst Flash (1x32Bit)
- 1 MBytes external asynchronous SRAM (2x16Bit) or

- up to 8 MBytes external synchronous SRAM (1x32Bit)

For the OnBoardMemory are reserved chip select 0 and 1. Therefore only two parts, e.g. 2x16Bit Flash and 2x16Bit asynchronous SRAM, should be assembled and can be used at the same time. Chip Select 2 and 3 are not used on the board and can be used externally.

The Board supports programming though the JTAG port (OCDS1).

4.4 FLASH

The flash uses 32 Data Bits (AD0...AD31) and 20, 21 or 22 Address Bits (A2...A21,A22 or A23). It's accessed via /CS0 or /CS1. Each type of flash has its own resistor to connect to /CS0 or /CS1. For connect the different flash see **Chapter 5.5**.

4.5 SRAM

The SRAM uses 32 Data Bits (AD0...AD31) and up to 22 Address Bits (A2...A22).

It's accessed via /CS0 or /CS1. Each type of SRAM has its own resistor to connect to /CS0 or /CS1. For connect the different SRAM see **Chapter 5.5**.

4.6 Peripherals

- The available peripherals on the TC1796 are
- System Timer
- General Purpose Timer Array V4 (GPTA0, GPTA1 and LTCA2)
- Asynchronous Serial Interface (ASC0 and ASC1)
- Synchronous Serial Interface (SSC0 and SSC1)
- MultiCAN (CAN0, CAN1, CAN2 and CAN3)
- Micro Second Bus Interface (MSC0 and MSC1)
- Micro Link Serial Bus Interface (MLI0 and MLI1)
- Analog Digital Converter (ADC0,ADC1 and FADC) with 44 analog inputs

4.7 ASC

There are two ASC interfaces possible. ASC0 is connected to the DB9 socket and ASC1 is connected to the BERG10 plug. ASC0 and ASC1 are driven via the RS232 Transceiver MAX3225. The DB9 socket can be connected to the serial port of a PC with a 1 to 1 RS232 cable.

To use the interfaces ASC0 and ASC1 via the plug X802 (without Transceiver) jumper JP401 (see **Table 5-2 "Jumper for ASC0" on Page 5-4**) and JP402 (see **Table 5-3 "Jumper for ASC1" on Page 5-4**) have to be changed (see **Figure 9-11**).

4.8 SSC

On the TC1796A there are two synchronous serial interfaces available but there is no special plug on board. To connect peripherals to SSC's the connector X802 (Peripherals) can be used.

The SSC0 of the TC1796A is connected to a serial EEPROM with a size of 128K (16.384 x 8). As chip select for this EEPROM is used the line SLSO0. To disable the EEPROM remove resistor R406.

4.9 MultiCAN

On the board are two CAN transceiver connected to the MultiCAN on TC1796 node 0 and 1. The transceivers are connected to two BERG10 plug. For the pinout of BERG10 plug see **Figure 8-8**.

The other two nodes (CAN2 and CAN3) can be use via plug X802. To use the CAN0 and CAN1 interfaces via the plug X802 (without Transceiver) remove resistors R409 and R410 and assemble R404 and R405 with a 0R resistor.

4.10 Other peripherals

For all other peripherals there are no special plugs on the board. The peripheral signals are available on the different connectors. See **"Connector Pin Assignment" on Page 8-1**.

Note: - SLSO0 is used as chip select for the serial eeprom on board.

4.11 Toggle LED

Port 1 pin 15 is connected to a single LED (D401) and can be controlled by Software. This status LED is low active.

4.12 Debug System

4.12.1 OCDS

The OCDS1 signals are connected to the BERG16 plug (X501). They work with the port supply of 3.3V.

The OCDS2 signals are connected to the SAMTEC HighSpeed plug (X502). They also work with the port supply of 3.3V.

The clock signal for OCDS1 and OCDS2 is always TRCLK (this clock must be enabled by software for using this clock).

4.12.2 On Board Wiggler

The On Board Wiggler is used to connect a PC to the TriBoard OCDS1 via the 5V parallel port.

The Wiggler can be enabled or disabled by setting the jumper JP501 (see **Table 5-4 "Jumper for On Board Wiggler" on Page 5-4** and **Figure 9-11**).

5 TriBoard Configuration

5.1 HW Boot Configuration

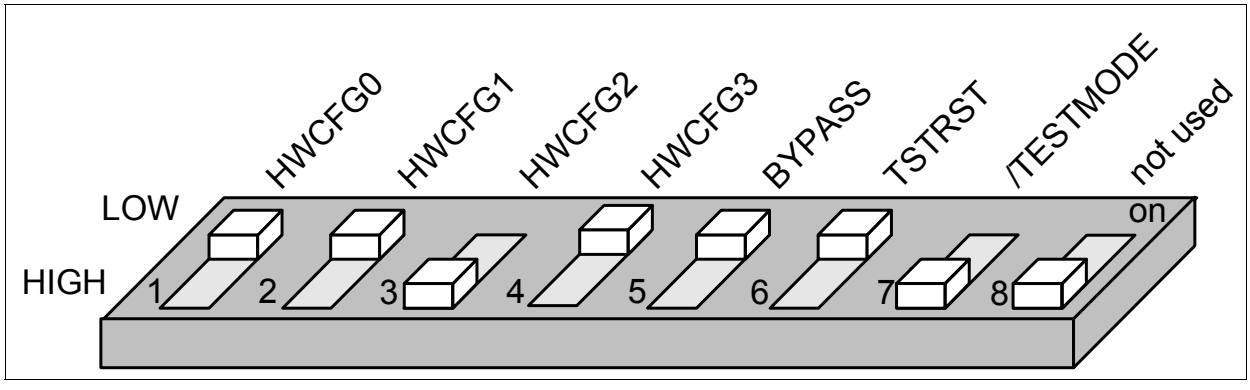

Figure 5-1 HW Configuration DIP-Switch

The picture above shows the definition of the boot HW configuration switch. The meaning of the switches will be described in the following table (**Table 5-1**).

Note: The ON position of the switch is equal to a logical LOW at the dedicated pin.

5.1.1 TC1796 HW Boot Configuration

Table 5-1 HW Boot Configuration for TC1796

Note: The shadowed line indicates the default setting.

Note: 'x' represents the don't care state.

Note: The signal /BRK_IN will be set by the Debugger via OCDS-Interface.

/BRK_IN	HWCFG[3...0]	Type of Boot	PC Start value
1	0000	Serial boot from ASC to PMI scratchpad, run loaded program	0xD4000000
1	0001	Serial boot from CAN to PMI scratchpad, run loaded program	0xD4000000
1	0010	Start from internal flash	0xA0000000
1	0011	Alternate Bootmode from internal flash	from Header or 0xD4000000
1	0100	External memory, EBU as master	0xA1000000
1	0101	Alternate Bootmode from External memory, EBU as master	from Header or 0xD4000000
1	0110	External memory, EBU as slave	0xA1000000
1	0111	Alternate Bootmode from External memory, EBU as slave	from Header or 0xD4000000
1	1XXX	reserved; don't use this combination	-
0	1000	go to external emulator space	0xDE000000
0	0000	put chip in tristate (deep sleep)	-
0	all others	reserved; don't use this combination	-

5.2 SW Boot Configuration

The TC1796 has 16 inputs (Port 0) which are latched with the /HRST signal. This latched value can be used as SW configuration. On the Bottomside (see **Figure 9-12**) from the TriBoard exist two Dipswitches which can be used for SW configuration. The Dipswitches connect the port inputs to ground via 1k resistor. The port has internal pullups. If the Dipswitch is closed the the corresponding bit is low otherwise high.

The following inputs are used by the bootrom software and should be used carefully:

P0.0, P0.1 and P0.2 are used by the Alternate Bootmode for selecting the Bootstraploader in case of not usable Alternate Boot.

P0.4 is used to disable flash accesses in the bootrom. In case of not functional flash of device make sure that switch 5 of S401 is ON. Normally this switch should be OFF. Is this switch is ON then the internal flash is not usable.

Refer to Users Manual TC1796 for more information.

All other pins can be used by your own software.

5.3 Clock Selection

The resulting CPU clock is:

- $f_{CPUCLK} = \frac{N}{PK} \cdot f_{OSC}$ without Bypass (switch is ON)
- $f_{CPUCLK} = f_{OSC}$ with Bypass (switch is OFF)

Note: The factors K, P and N are controlled via bitfields in register PLL_CLC located in the SCU.

The resulting system clock is:

- $f_{SYSTEMCLK} = \frac{f_{CPUCLK}}{2}$ if SYSFS cleared (default after reset)
- $f_{SYSTEMCLK} = f_{CPUCLK}$ if SYSFS is set

Note: The bit SYSFS is controlled via bit 2 in register PLL_CLC located in the SCU.

5.4 Jumper Settings.

Table 5-2 Jumper for ASC0

Note: The shadowed line indicates the default setting

Setting	ASC0 Configuration
1 - 2	Transceiver --> CPU
2 - 3	ext. RxD --> CPU

Table 5-3 Jumper for ASC1

Note: The shadowed line indicates the default setting

Setting	ASC1 Configuration
1 - 2	Transceiver --> CPU
2 - 3	ext. RxD --> CPU

Table 5-4 Jumper for On Board Wiggler

Note: The shadowed line indicates the default setting

Setting	On Board Wiggler
1 - 2	Enable On Board Wiggler
2 - 3	Disable On Board Wiggler

5.5 Optional Resistors

Table 5-5 Resistors for XTAL1 Operation

R314	use XT301 (default: short)
R315	Rserial (default: short)
R316	Rparallel (default: open)

Table 5-6 Resistors for flash AM29BL162C

R212	use /CS0 (default: short)
R213	use /CS1 (default: open)
R214	pullup on chip select the device (default: open)

Table 5-7 Resistors for 32 bit flash

R218	use /CS0 (default: open)
R219	use /CS1 (default: open)
R220	pullup on chip select the device (default: open)

Table 5-8 Resistors for other 16 bit flash

R215	use /CS0 (default: open)
R216	use /CS1 (default: open)
R217	pullup on chip select the device (default: open)

Table 5-9 Resistors for asynchronous SRAM

R122	use /CS0 (default: open)
R121	use /CS1 (default: short)
R123	pullup on chip select the device (default: open)

Table 5-10 Resistors for synchronous SRAM

R125	use /CS0 (default: open)
R124	use /CS1 (default: open)
R126	pullup on chip select the device (default: open)

6 TriBoard Software

6.1 Requirements

To install the software from your TriBoard CD you need a PC with Windows95/98/ME, WindowsNT4.0 or Windows 2000.

6.2 Software Overview

The CD does not contain any tool. For the availablity for Demo Versions of the different Tools, please contact the toolvendor directly (e.g. Tasking, Hitex, Lauterbach, GreenHills, HighTec...). To install tools for compiling and debugging use seperat CD's from Toolvendors. There are also some application notes and software examples. The directory "Schematics" contains libraries and some examples of extension boards in the Protel file format. The data sheets of all used parts can be found in the "TriBoard_Components" directory. The manuals for the microcontrollers and the TriBoard are located in the "Manual" folder. Some useful tools like Acrobat Reader are stored in the "Utilities" directory.

The current Errata Sheet can be found in the directory "Errata Sheet". To make sure you have always the most recent one, please contact your local FAE.

Note: For more details see the file ReadMe.txt.

6.3 Software Installation

To install tools for the TriCore insert the CD from the Toolvendor and start the file "setup.exe" if the CD is not automatically started. Follow the instructions of the installationprogram.

7 Signal Description

For more information about the signals please see the user manuals from TC1796.

Table 7-1 Power Signals

Short Name	Description
VCC_IN	Supply Input (5,5V...60V)
GND	Ground
VDD	Core Supply Voltage (1.5V)
VDDP	Port Supply Voltage (3.3V)
VDDEBU	External Bus Supply Voltage (2.5V or 3.3V)
VDDFL3	Flash Supply Voltage (3.3V)
VDDSBRAM	SRAM standby Supply Voltage (1.5V)
VDDOSC	Main Oscillator Supply Voltage (1.5V)
VDDOSC3	Main Oscillator Supply Voltage (3.3V)
VSSOSC	Main Oscillator Ground
VSSM	ADC0/1 Analog Part Ground
VDDM	ADC0/1 Analog Part Supply Voltage
VSSMF	FADC Analog Part Ground
VDDMF	FADC Analog Part Supply Voltage
VAGND0	ADC0 Reference Ground
VAREF0	ADC0 Reference Voltage
VAGND1	ADC1 Reference Ground
VAREF1	ADC0 Reference Voltage
VFAGND	FADC Reference Ground
VFAREF	FADC Reference Voltage

Table 7-2 Reset Signals

Short Name	Description
/PORST	External Power On Reset
/HDRST	Hardware Reset
TSTRES	Test Reset

Table 7-3 Interrupt Signals

Short Name	Description
/NMI	Non Maskable Interrupt
REQ[0...7]	External Trigger Input 0...7

Table 7-4 Clock Signals

Short Name	Description
XTAL1	Crystal Oscillator Input
XTAL2	Crystal Oscillator Output
BFCLKO	Burst Mode Flash Clock Output
BFCLKI	Burst Mode Flash Clock Input

Table 7-5 BUS Signals

Short Name	Description
D[0...31]	Data Bus
A[0...23]	Address Bus

Table 7-6 BUS Control Signals

Short Name	Description
/CS[0...3]	Chip Selects
/CSCOMB	Combined Chip Select Output
/BC[0...3]	Byte Controls
/RD	Read
/WR	Write
MR/W	Motorola-style Read/Write
/BAA	Burst address advance output
/ADV	Address Valid
/BREQ	Bus Request Output
/HOLD	Hold Request Input
/HLDA	Hold Acknowledge
/WAIT	Wait Input

Table 7-7 Debug Signals

Short Name	Description
/TRST	Test Reset
TCLK	Test Clock
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
TRCLK	Trace Clock for OCDS Level 2
TESTMODE	Test Mode Select Input
/BRK_IN	TriCore Breakpoint Input
BYPASS	Bypass PLL
/BRK_OUT	TriCore Breakpoint Output
BRKPT[0...2]	TriCore Breakpoint (TR5..7)
STATUS[0...4]	TriCore Status (TR0..4)
IND_PC[0...7]	TriCore Indirect Program Counter (TR8..15)

Table 7-8 Peripheral Signals

Short Name	Description
RXD0	Receive Data ASC0
RXD0_EXT	Receive Data ASC0 (see Table 5.3)
TXD1	Transmit Data ASC1
RXD1_EXT	Receive Data ASC1 (see Table 5.3)
SCLK0	Clock Line SSC0
MRST0	Master Receive / Slave Transmit SSC0
MTSR0	Master Transmit / Slave Receive SSC0
SLSI0	Slave Select Input SSC0
SLSO0	Slave Select Output 0 (SSC0)
SLSO1	Slave Select Output 1 (SSC0)
SCLK1	Clock Line SSC1
MRST1	Master Receive / Slave Transmit SSC1
MTSR1	Master Transmit / Slave Receive SSC1
SLSI1	Slave Select Input SSC1
SLSO[2..7]	Slave Select Output 2..7

Table 7-8 Peripheral Signals

TXCAN0	CAN Transmitter Output 0
RXCAN0	CAN Receiver Input 0
TXCAN1	CAN Transmitter Output 1
RXCAN1	CAN Receiver Input 1
TXCAN2	CAN Transmitter Output 2
RXCAN2	CAN Receiver Input 2
TXCAN3	CAN Transmitter Output 3
RXCAN3	CAN Receiver Input 3
GPTUA [0...55]	General Purpose Timer Array
P0 [0...15]	General Purpose I/O Port 0 (SWOPT)
P1[12...15]	General Purpose I/O Port 1.12...1.15
AN[0...43]	Analog Inputs
AD0EMUX[0...1]	ADC0 External Multiplexer Control
AD1EMUX[0...1]	ADC1 External Multiplexer Control
FCLP0A	MSC0 differential driver clock output positive A
FCLN0	MSC0 differential driver clock output negative
SOP0A	MSC0 differential driver serial data output positive A
SON0	MSC0 differential driver serial data output negative
EN00	MSC0 device select output 0
SDI0	MSC0 serial data input
FCLP1A	MSC1 differential driver clock output positive A
FCLN1	MSC1 differential driver clock output negative
SOP1A	MSC1 differential driver serial data output positive A
SON1	MSC1 differential driver serial data output negative
EN10	MSC1 device select output 0
SDI1	MSC1 serial data input
RCLK0	MLI0 receive channel clock
RREADY0	MLI0 receive channel ready output
RVALID0	MLI0 receive channel valid input
RDATA0	MLI0 receive channel data input
TCLK0	MLI0 transmit channel clock

Table 7-8 Peripheral Signals

TREADY0	MLI0 transmit channel ready input
TVALID0	MLI0 transmit channel valid output
TDATA0	MLI0 transmit channel data output
P10[0...3]	General Purpose I/O Port 10 (used as HWCFG)

8 Connector Pin Assignment

The TriBoard will be shipped with four male (plug) connectors on top layer and four female (socket) connectors on bottom layer. The default connectors are 80-pol. Board to Board connectors from Samtec:

http://www.samtec.com

Plug:Socket:

FTSH-140-02-L-DV-ES-AFLE-140-01-G-DV-A

Alternative there can be used the Board to Board System from Robinson Nugent:

http://www.robinsonnugent.com

Plug:Socket:

P50L-80P-AS-TGFP50L-80S-AS-TGF

8.1 TC1796 Connector / Top View

BUS EXPANSION (X801,X901)				PERIPHERALS (X802,X902)			
GND	1	2	GND	GND	1	2	GND
GND	3	4	GND	GND	3	4	GND
D0	5	6	A0	VCC_IN	5	6	VCC_IN
D1	7	8	A1	VCC_IN	7	8	VCC_IN
D2	9	10	A2	/ADV	9	10	/BAA
D3	11	12	A3	BFCLKO	11	12	BCK
D4	13	14	A4	P0.5	13	14	/BCK
D5	15	16	A5	/NMI	15	16	/HDRST
D6	17	18	A6	DSQ0	17	18	DSQ1
D7	19	20	A7	GND	19	20	GND
D8	21	22	A8	P0.6	21	22	/PORST
D9	23	24	A9	P0.7	23	24	P0.8
D10	25	26	A10	EN00 / P5.4	25	26	EN10 / P5.6
D11	27	28	A11	SDI0 / P5.5	27	28	SDI1 / P5.7
D12	29	30	A12	FCLP0A	29	30	FCLP1A
D13	31	32	A13	FCLN0	31	32	FCLN1
D14	33	34	A14	SOP0A	33	34	SOP1A
D15	35	36	A15	SON0	35	36	SON1
D16	37	38	A16	RXCAN3 / P6.14	37	38	TXCAN3 / P6.15
D17	39	40	A17	SLSI0	39	40	SLSI1
D18	41	42	A18	SLSO0	41	42	SLSO1
D19	43	44	A19	SLSO2 / P2.2	43	44	SLSO3 / P2.3
D20	45	46	A20	SLSO4 / P2.4	45	46	SLSO5 / P2.5
D21	47	48	A21	SLSO6 / P2.6	47	48	SLSO7 / P2.7
D22	49	50	A22	GND	49	50	GND
D23	51	52	A23	XTAL1	51	52	SYSCLK / P1.12
D24	53	54		XTAL2	53	54	BFCLKI
D25	55	56		RXD0_EXT / P5.0	55	56	RXD1_EXT / P5.2
D26	57	58	/CS2	TXD0 / P5.1	57	58	TXD1 / P5.3
D27	59	60	/CS1	RXCAN0 / P6.8	59	60	RXCAN1 / P6.10
D28	61	62	/CS0	TXCAN0 / P6.9	61	62	TXCAN1 / P6.11
D29	63	64	/BC3	SCLK0	63	64	SCLK1 / P6.6
D30	65	66	/BC2	MTSR0	65	66	MTSR1 / P6.4
D31	67	68	/BC1	MRST0	67	68	MRST1 / P6.5
/RD	69	70	/BC0	RXCAN2 / P6.12	69	70	TXCAN2 / P6.13
/WR	71	72	/CSCOMB	REQ0 / P1.0	71	72	REQ1 / P1.1
MRW	73	74		REQ2 / P1.2	73	74	REQ3 / P1.3
/HLDA	75	76	/WAIT	VDDSBRAM	75	76	GND
	77	78	/BREQ	3V3	77	78	VDDE
/HOLD	79	80	/CS3	3V3	79	80	VDDE

Figure 8-1 Connector for TC1796 - Pinout (Part I, Top View)

ADC (X803, X903)

VSSA	1	2	VSSA
VSSA	3	4	VSSA
AN0	5	6	AN16
AN1	7	8	AN17
AN2	9	10	AN18
AN3	11	12	AN19
AN4	13	14	AN20
AN5	15	16	AN21
AN6	17	18	AN22
AN7	19	20	AN23
AN8	21	22	AN24
AN9	23	24	AN25
AN10	25	26	AN26
AN11	27	28	AN27
AN12	29	30	AN28
AN13	31	32	AN29
AN14	33	34	AN30
AN15	35	36	AN31
VSSA	37	38	VSSA
VDDM	39	40	VDDMF
VSSFAREF	41	42	VDDFAREF
VSSAREF0	43	44	VSSAREF1
VDDAREF0	45	46	VDDAREF1
VSSA	47	48	VSSA
AN32	49	50	AN38
AN33	51	52	AN39
AN34	53	54	AN40
AN35	55	56	AN41
AN36	57	58	AN42
AN37	59	60	AN43
VSSA	61	62	VSSA
P0.8	63	64	P0.9
P0.10	65	66	P0.11
P0.12	67	68	P0.13
3V3	69	70	VDDE
AD0EMUX0 / P7.2	71	72	AD1EMUX0 / P7.6
AD0EMUX1 / P7.3	73	74	AD1EMUX1 / P7.7
REQ5 / P7.1	75	76	P0.14
P0.15	77	78	REQ4 / P7.0
REQ7 / P7.5	79	80	REQ6 / P7.4

GPTA / MLI (X804,X904)

GND	1	2	GND
GND	3	4	GND
GPTA0 / P2.8	5	6	GPTA32 / P4.8
GPTA1 / P2.9	7	8	GPTA33 / P4.9
GPTA2 / P2.10	9	10	GPTA34 / P4.10
GPTA3 / P2.11	11	12	GPTA35 / P4.11
GPTA4 / P2.12	13	14	GPTA36 / P4.12
GPTA5 / P2.13	15	16	GPTA37 / P4.13
GPTA6 / P2.14	17	18	GPTA38 / P4.14
GPTA7 / P2.15	19	20	GPTA39 / P4.15
GPTA8 / P3.0	21	22	GPTA40 / P8.0
GPTA9 / P3.1	23	24	GPTA41 / P8.1
GPTA10 / P3.2	25	26	GPTA42 / P8.2
GPTA11 / P3.3	27	28	GPTA43 / P8.3
GPTA12 / P3.4	29	30	GPTA44 / P8.4
GPTA13 / P3.5	31	32	GPTA45 / P8.5
GPTA14 / P3.6	33	34	GPTA46 / P8.6
GPTA15 / P3.7	35	36	GPTA47 / P8.7
GPTA16 / P3.8	37	38	GPTA48 / P9.0
GPTA17 / P3.9	39	40	GPTA49 / P9.1
GPTA18 / P3.10	41	42	GPTA50 / P9.2
GPTA19 / P3.11	43	44	GPTA51 / P9.3
GPTA20 / P3.12	45	46	GPTA52 / P9.4
GPTA21 / P3.13	47	48	GPTA53 / P9.5
GPTA22 / P3.14	49	50	GPTA54 / P9.6
GPTA23 / P3.15	51	52	GPTA55 / P9.7
GPTA24 / P4.0	53	54	P9.8
GPTA25 / P4.1	55	56	P10.0
GPTA26 / P4.2	57	58	EMGSTOP / P10.1
GPTA27 / P4.3	59	60	P10.2
GPTA28 / P4.4	61	62	P10.3
GPTA29 / P4.5	63	64	P1.13
GPTA30 / P4.6	65	66	P1.14
GPTA31 / P4.7	67	68	P1.15
TCLK0 / P1.4	69	70	RDATA0 / P1.11
TREADY0 / P1.5	71	72	RVALID0 / P1.10
TVALID0 / P1.6	73	74	RREADY0 / P1.9
TDATA0 / P1.7	75	76	RCLK0 / P1.8
3V3	77	78	VDDE
3V3	79	80	VDDE

Figure 8-2 Connector for TC1796 - Pinout (Part II, Top View)

8.2 General Connector / Top View

The general connector is defined as an standard for future releases of boards like the TriBoard. There have been borne in mind yet another TriCore based CPUs.

BUS EXPANSION (X801,X901)				PERIPHERALS / OCDS (X802,X902)			
GND	1	2	GND	GND	1	2	GND
GND	3	4	GND	GND	3	4	GND
AD0	5	6	A0	VCC_IN	5	6	VCC_IN
AD1	7	8	A1	VCC_IN	7	8	VCC_IN
AD2	9	10	A2	/ADV	9	10	/BAA
AD3	11	12	A3	EBUCLK_OUT	11	12	/CODE
AD4	13	14	A4	/CSEMU	13	14	/CSOVL
AD5	15	16	A5	/NMI	15	16	/HRST
AD6	17	18	A6	SVM	17	18	VDDFLT
AD7	19	20	A7	GND	19	20	GND
AD8	21	22	A8	/TRST	21	22	/PORST
AD9	23	24	A9	TCLK	23	24	STATUS0
AD10	25	26	A10	TMS	25	26	STATUS1
AD11	27	28	A11	TDI	27	28	STATUS2
AD12	29	30	A12	TDO	29	30	STATUS3
AD13	31	32	A13	/OCDS_E	31	32	STATUS4
AD14	33	34	A14	/BRK_IN	33	34	/TESTMODE
AD15	35	36	A15	/BRK_OUT	35	36	SCAN_E
AD16	37	38	A16	FT-ANALOG	37	38	BRKPT0
AD17	39	40	A17	BRKPT1	39	40	BRKPT2
AD18	41	42	A18	IND_PC0	41	42	IND_PC1
AD19	43	44	A19	IND_PC2	43	44	IND_PC3
AD20	45	46	A20	IND_PC4	45	46	IND_PC5
AD21	47	48	A21	IND_PC6	47	48	IND_PC7
AD22	49	50	A22	GND	49	50	GND
AD23	51	52	A23	XTAL1	51	52	XTAL3
AD24	53	54	A24	XTAL2	53	54	EBUCLK_IN
AD25	55	56	A25	RXD0_EXT	55	56	RXD1_EXT
AD26	57	58	/CS2	TXD0	57	58	TXD1
AD27	59	60	/CS1	RXCAN0	59	60	RXCAN1
AD28	61	62	/CS0	TXCAN0	61	62	TXCAN1
AD29	63	64	/BC3	SCLK0	63	64	SCLK1
AD30	65	66	/BC2	MTSR0	65	66	MTSR1
AD31	67	68	/BC1	MRST0	67	68	MRST1
/RD	69	70	/BC0	RXJ1850	69	70	TXRJ1850
/WR	71	72	ALE	P13.12	71	72	P13.13
/RAS	73	74	/CAS	P13.14	73	74	P13.15
/HLDA	75	76	/WAIT	VDDSTBY	75	76	GND
/CSFPI	77	78	/BREQ	VDDPERI	77	78	VDDBUS
/HOLD	79	80	/CS3	VDDPERI	79	80	VDDBUS

Figure 8-3 General Connector - Pinout (Part I, Top View)

ADC / GPIO (X803, X903)

VSSA	1	2	VSSA	
VSSA	3	4	VSSA	
AN0	5	6	AN16	
AN1	7	8	AN17	
AN2	9	10	AN18	
AN3	11	12	AN19	
AN4	13	14	AN20	
AN5	15	16	AN21	
AN6	17	18	AN22	
AN7	19	20	AN23	
AN8	21	22	AN24	
AN9	23	24	AN25	
AN10	25	26	AN26	
AN11	27	28	AN27	
AN12	29	30	AN28	
AN13	31	32	AN29	
AN14	33	34	AN30	
AN15	35	36	AN31	
VSSA	37	38	VSSA	
VDDA2	39	40	VDDA2	
VDDA2	41	42	VDDA2	
VSSAREF0	43	44	VSSAREF1	
VDDAREF0	45	46	VDDAREF1	
GND	47	48	GND	
GPTU1.0	49	50	GPTU1.1	
GPTU1.2	51	52	GPTU1.3	
GPTU1.4	53	54	GPTU1.5	
GPTU1.6	55	56	GPTU1.7	
PCP_PC0	57	58	PCP_PC1	
PCP_PC2	59	60	PCP_PC3	
PCP_PC4	61	62	PCP_PC5	
PCP_PC6	63	64	PCP_PC7	
PCP_PC8	65	66	P2.0	
/PCP_BRK_O	67	68	PCP_PC_OR	
VDDPERI	69	70	VDDBUS	
AD0EMUX0	71	72	AD1EMUX0	
AD0EMUX1	73	74	AD1EMUX1	
AD0EMUX2	75	76	AD1EMUX2	
AD0EXTIN0	77	78	AD0EXTIN1	
AD1EXTIN0	79	80	AD1EXTIN1	

GPTU / GPTA (X804,X904)

GND	1	2	GND	
GND	3	4	GND	
GPTA0	5	6	GPTA32	
GPTA1	7	8	GPTA33	
GPTA2	9	10	GPTA34	
GPTA3	11	12	GPTA35	
GPTA4	13	14	GPTA36	
GPTA5	15	16	GPTA37	
GPTA6	17	18	GPTA38	
GPTA7	19	20	GPTA39	
GPTA8	21	22	GPTA40	
GPTA9	23	24	GPTA41	
GPTA10	25	26	GPTA42	
GPTA11	27	28	GPTA43	
GPTA12	29	30	GPTA44	
GPTA13	31	32	GPTA45	
GPTA14	33	34	GPTA46	
GPTA15	35	36	GPTA47	
GPTA16	37	38	GPTA48	
GPTA17	39	40	GPTA49	
GPTA18	41	42	GPTA50	
GPTA19	43	44	GPTA51	
GPTA20	45	46	GPTA52	
GPTA21	47	48	GPTA53	
GPTA22	49	50	GPTA54	
GPTA23	51	52	GPTA55	
GPTA24	53	54	GPTA56	
GPTA25	55	56	GPTA57	
GPTA26	57	58	GPTA58	
GPTA27	59	60	GPTA59	
GPTA28	61	62	GPTA60	
GPTA29	63	64	GPTA61	
GPTA30	65	66	GPTA62	
GPTA31	67	68	GPTA63	
GPTU0.0	69	70	GPTU0.4	
GPTU0.1	71	72	GPTU0.5	
GPTU0.2	73	74	GPTU0.6	
GPTU0.3	75	76	GPTU0.7	
VDDPERI	77	78	VDDBUS	
VDDPERI	79	80	VDDBUS	

Figure 8-4 General Connector - Pinout (Part II, Top View)

8.3 Power Connector Pinout

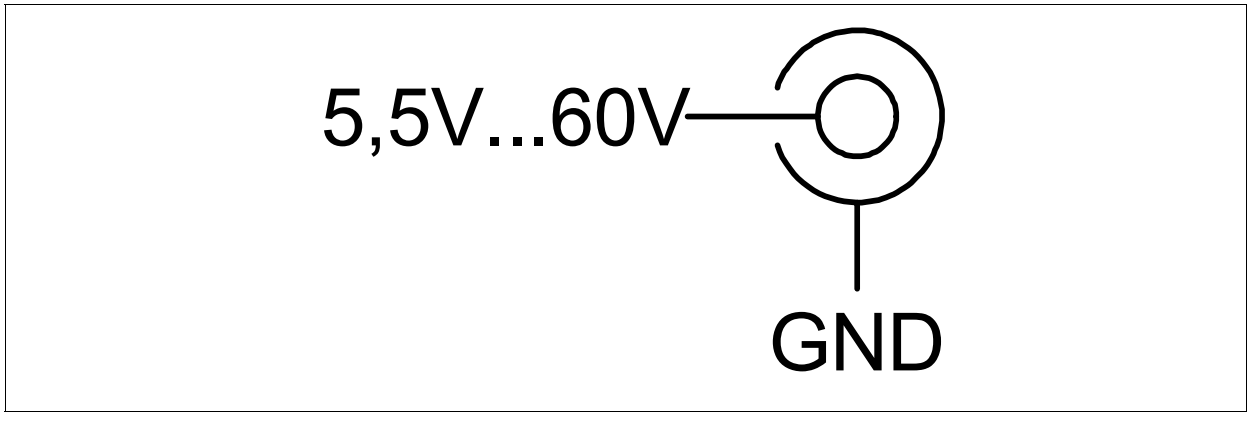

Figure 8-5 Power Connector Pinout

8.4 RS232 Pinout

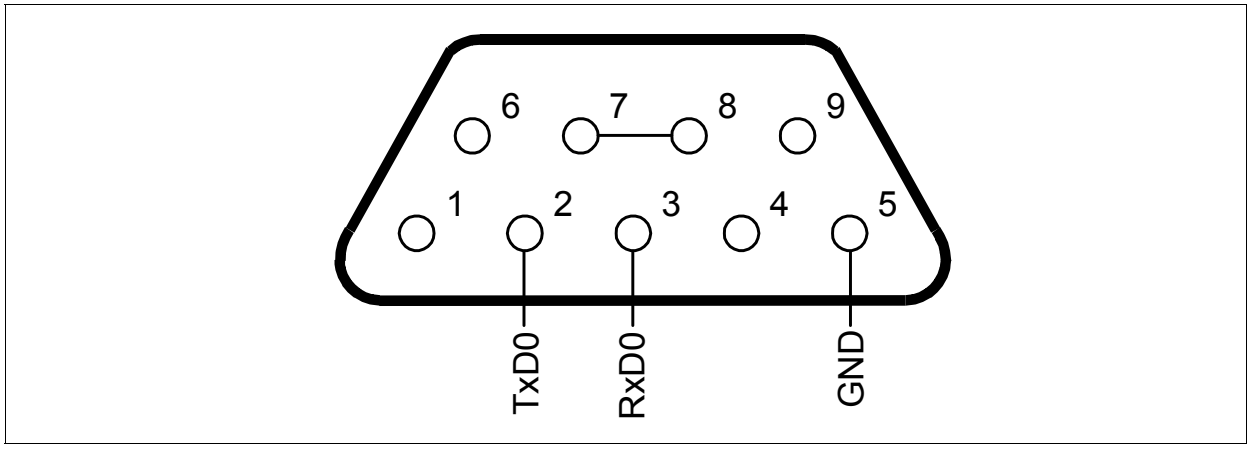

Figure 8-6 RS232-0 Pinout (DB9)

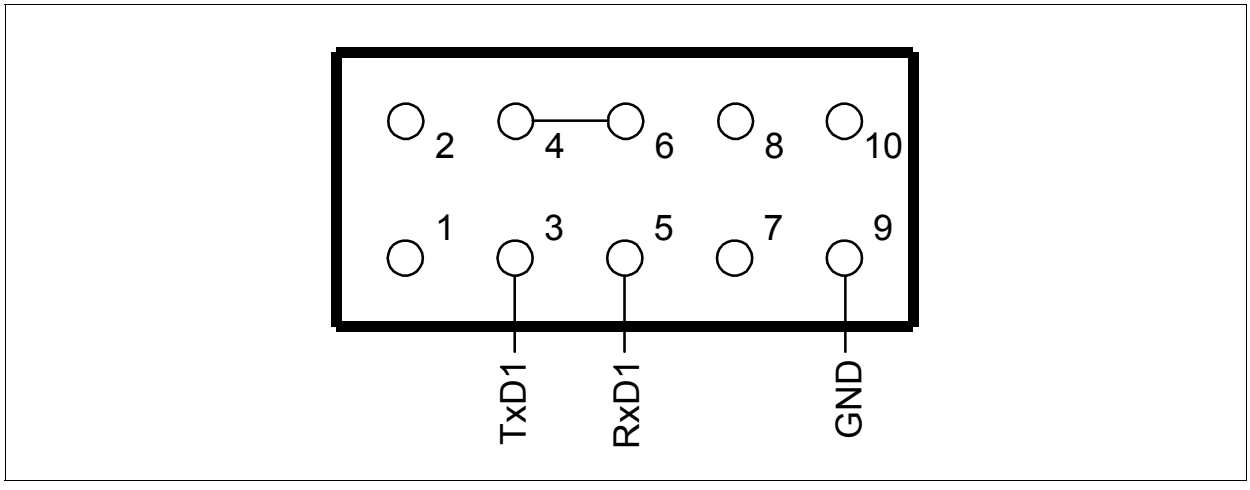

Figure 8-7 ASC1 Pinout (BERG10)

8.5 CAN Pinout

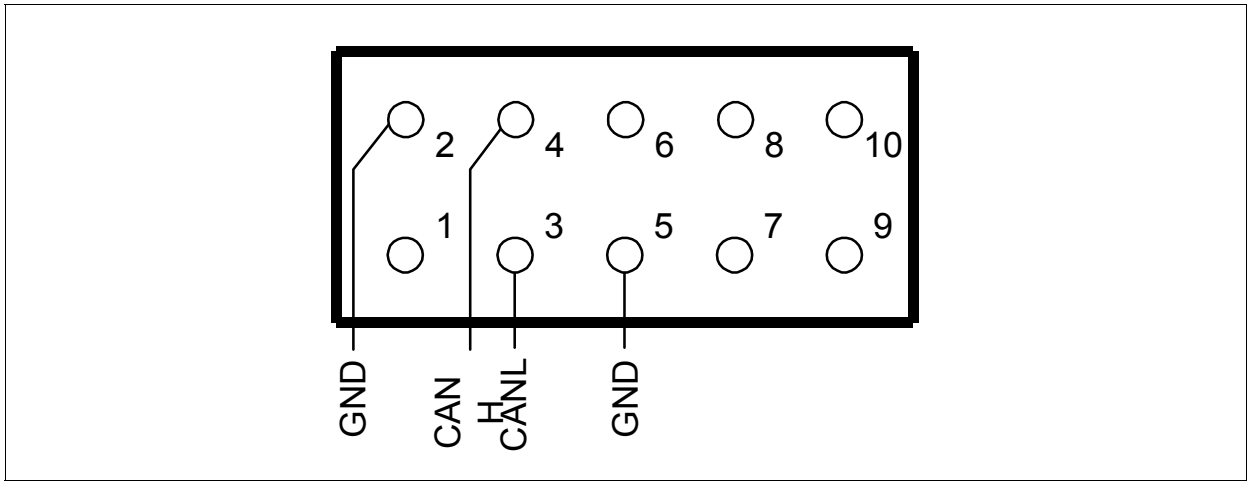

Figure 8-8 CAN Pinout (BERG10)

8.6 OCDS Pinout

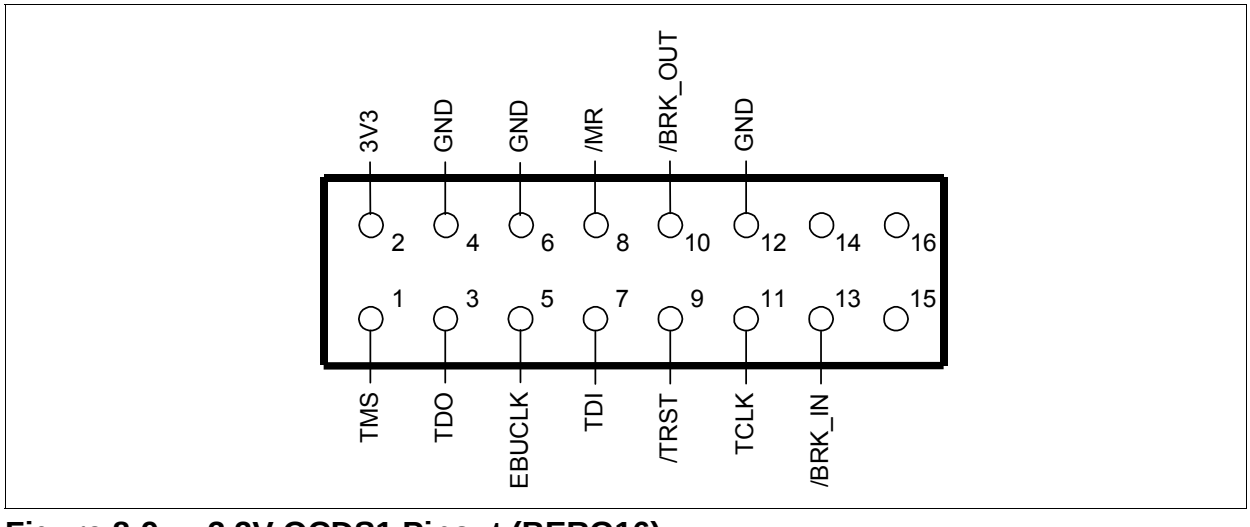

Figure 8-9 3.3V OCDS1 Pinout (BERG16)

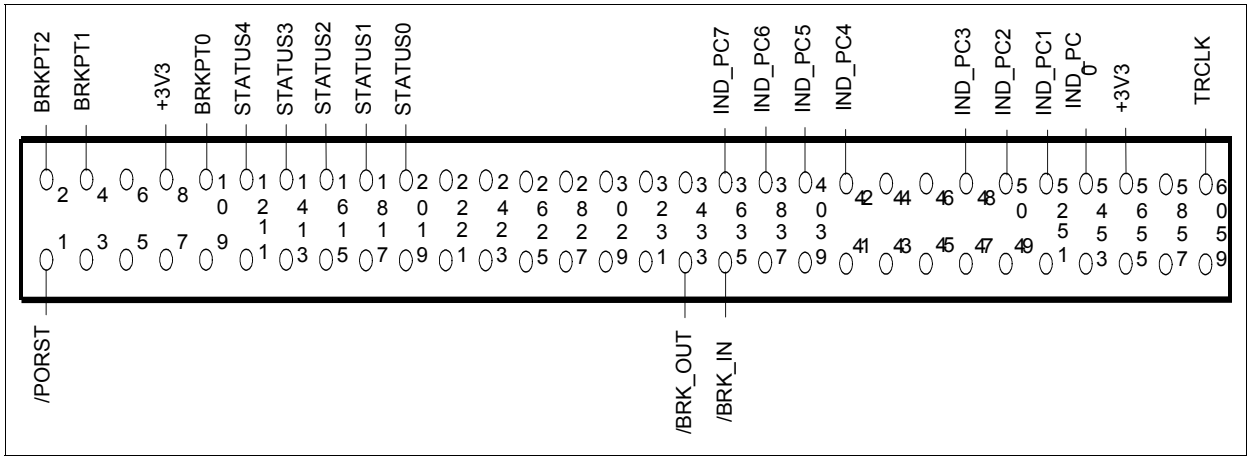

Figure 8-10 3.3V OCDS2 Pinout (SAMTEC QSH)

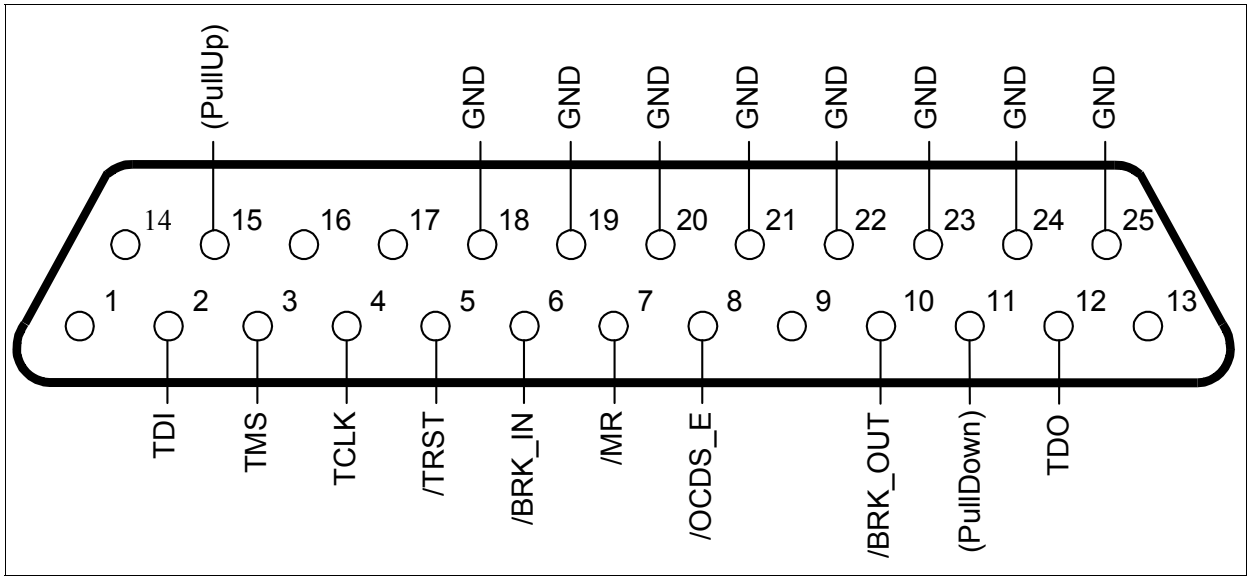

Figure 8-11 On Board Wiggler Pinout (DB25)

9 Schematic and Layout

9.1 Schematic

9.1.1 Know bugs and problems on the TriBoard TC1796.300

- First devices need higher core supply (1,7V)

  Solution:Assemble 15K for R715

  This is done on each TriBoard. For 1,5V core supply assemble R715 with 8,2K resistor.

- For using TriBoard with an Emulation Device, please check/change the following:
  1. Remove D502 and/or D503 if assembled
  2. Remove R526 and R527 if not 0R resistors and assemble 0R resistors
  3. For A-Step only: Remove R525
  4. For B-Step only: Remove 3,3V connection on R525 and connect R525 to EP1_10 (X503 pin 20)
  5. Remove XT501 if assembled
  6. Remove R529 if assembled
  7. Assemble R530 with 0R resistor if not assembled
  8. Remove R531 if assembled
  9. For A-Step only: Assemble R528 with 0R resistor if not assembled
  10. For B-Step only: Remove R528 if assembled, connect ETESTCNTRL and +1V5 (connect pin 31 and 33 of X503)

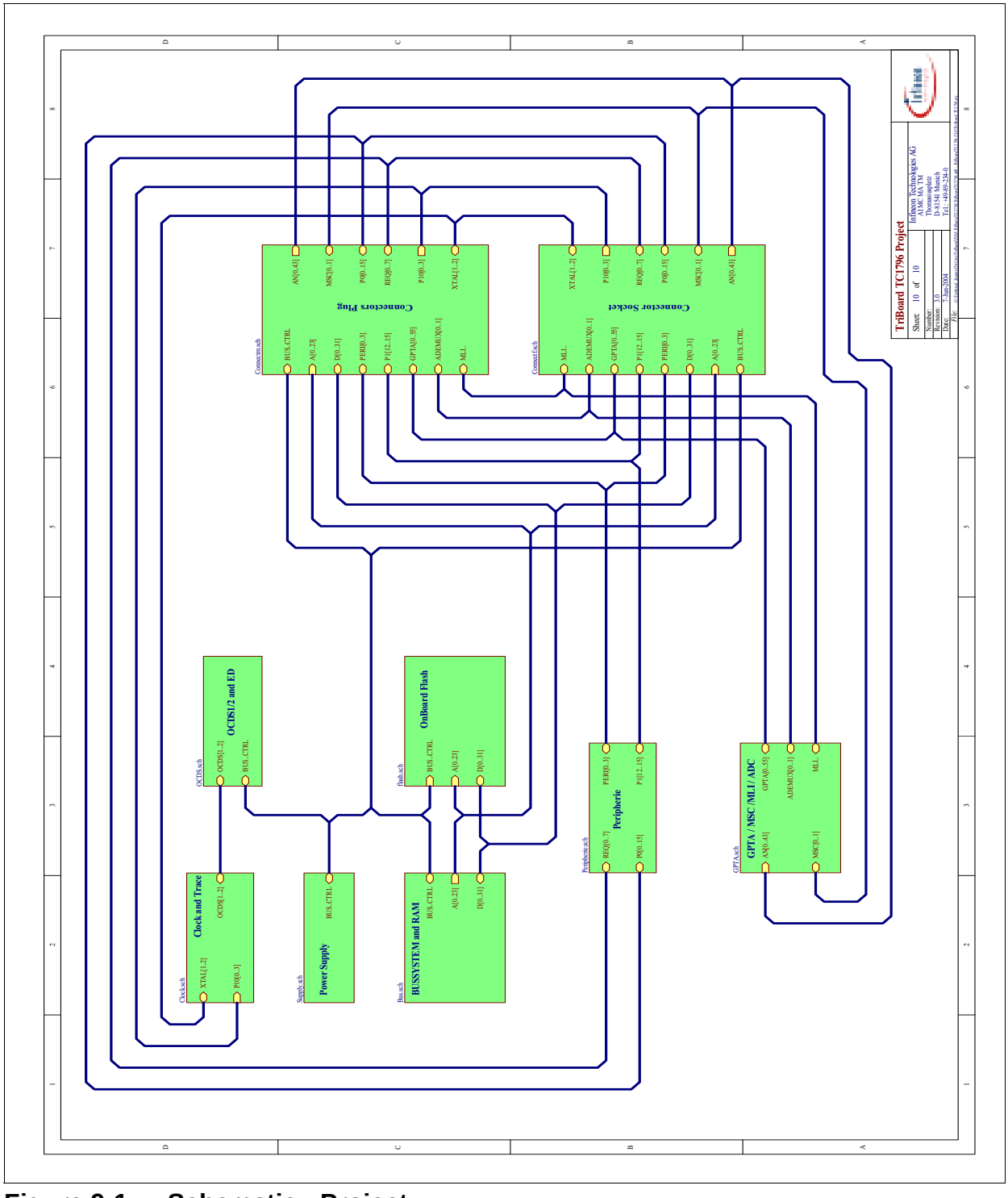

Figure 9-1 Schematic - Project

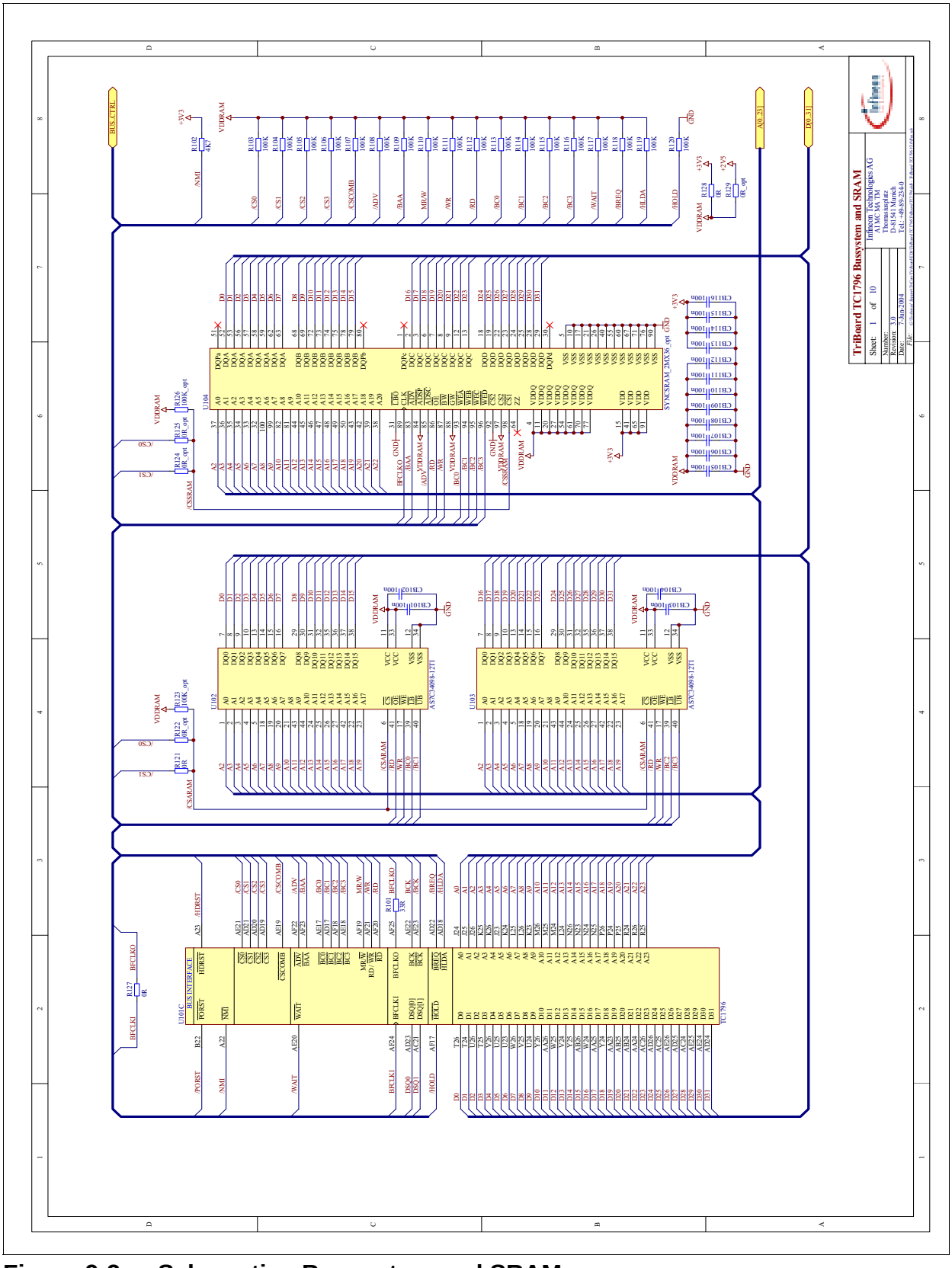

Figure 9-2 Schematic - Bussystem and SRAM

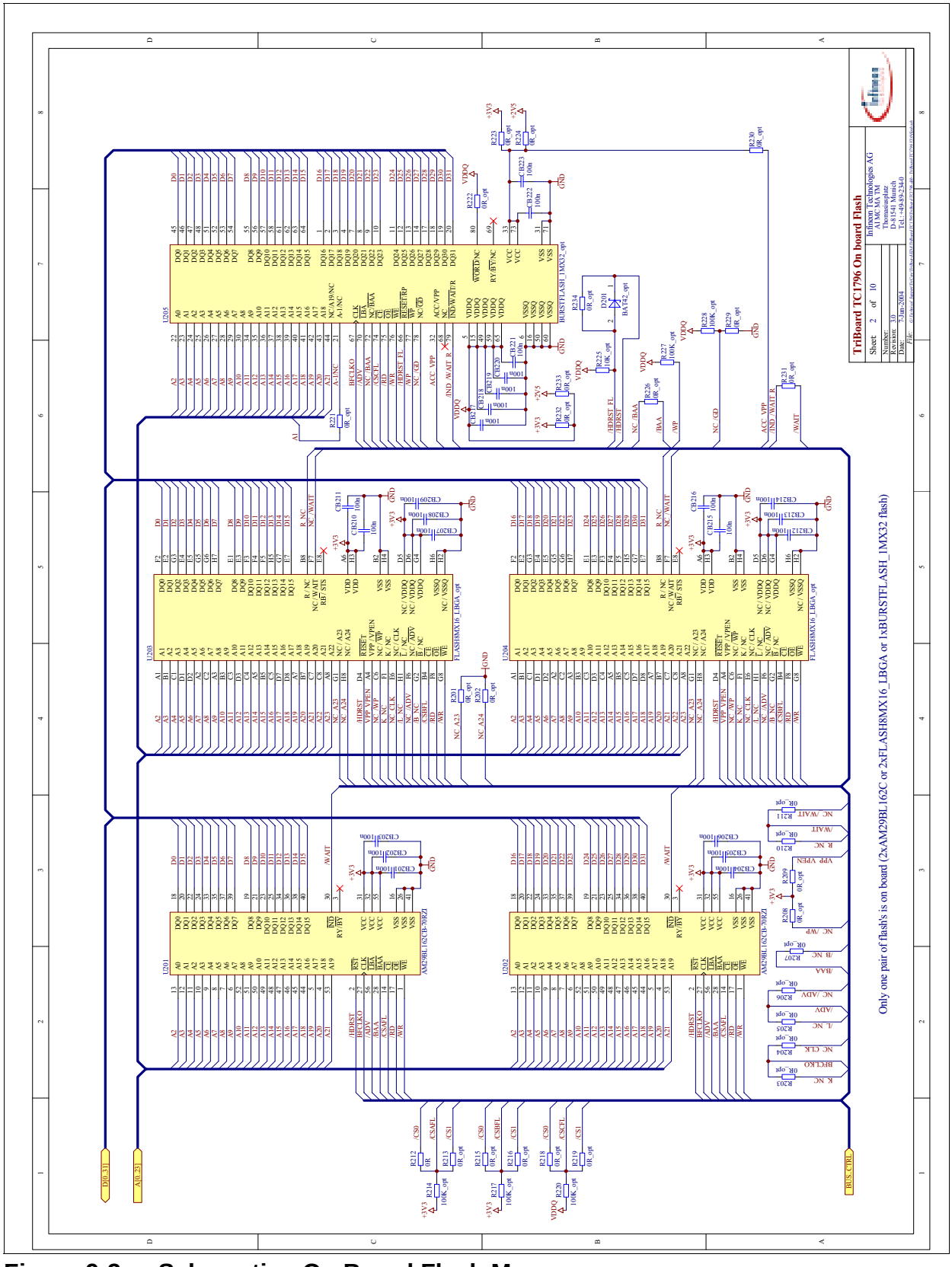

Figure 9-3 Schematic - On Board Flash Memory

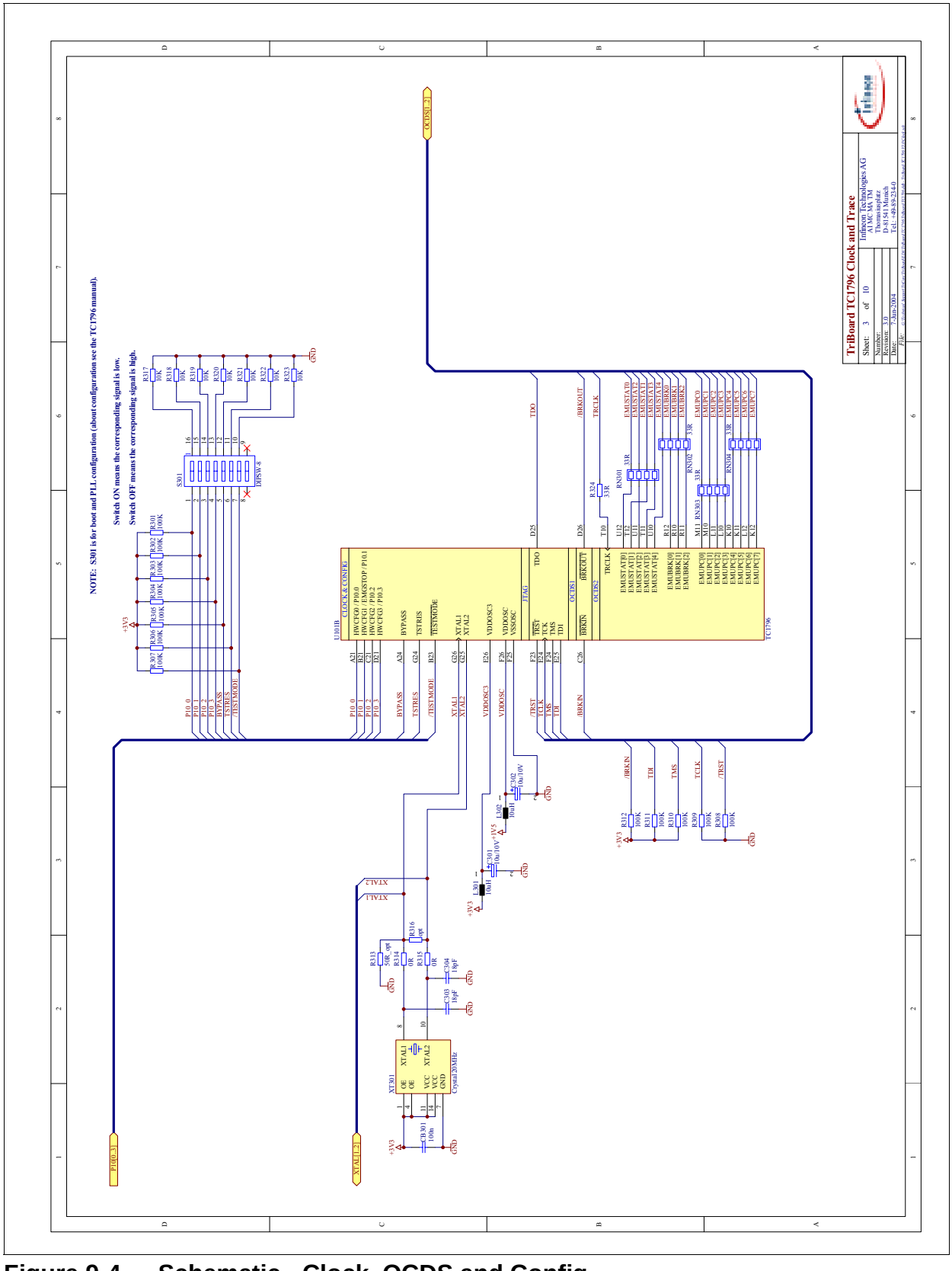

Figure 9-4 Schematic - Clock, OCDS and Config

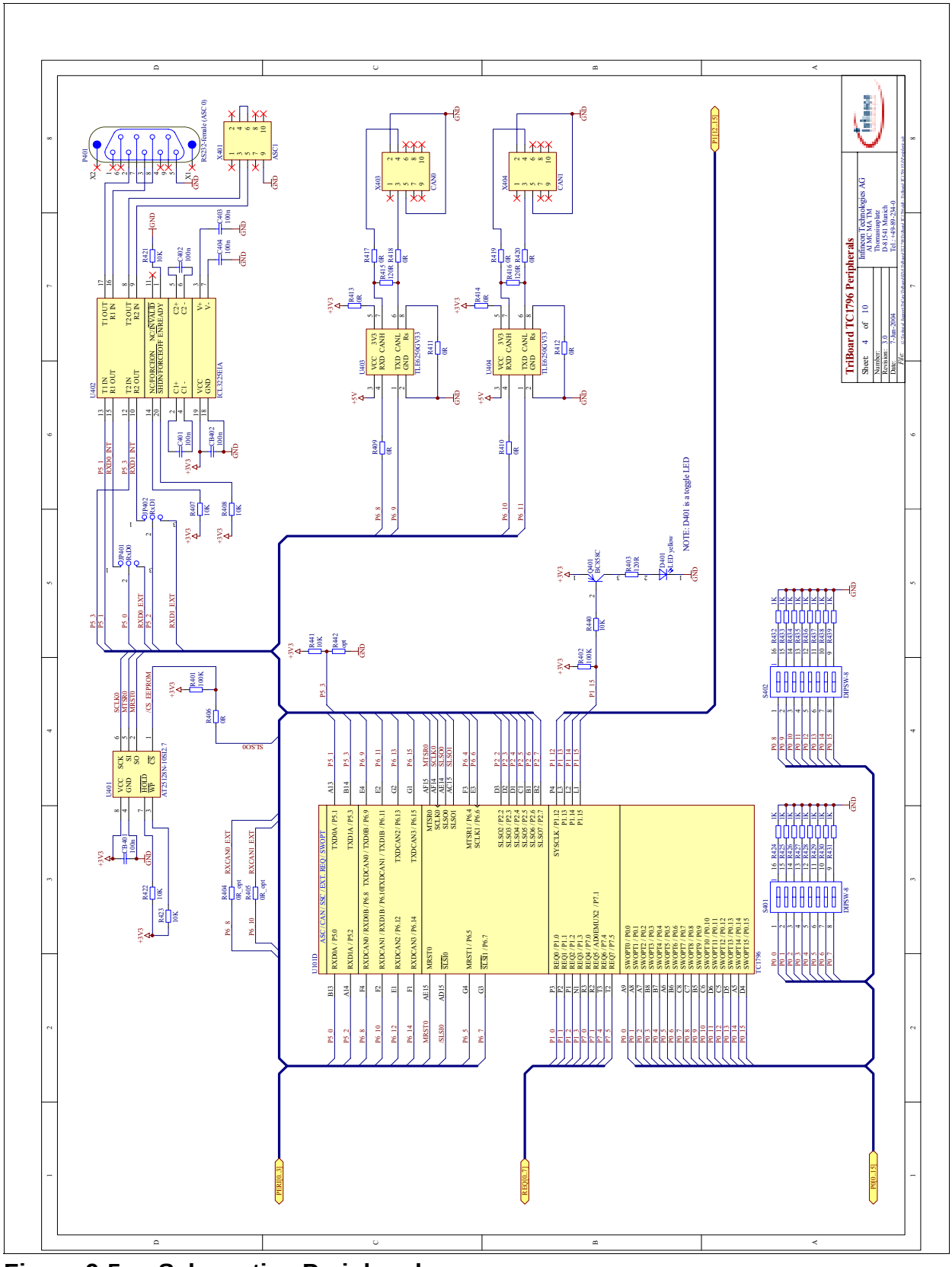

Figure 9-5 Schematic - Peripherals

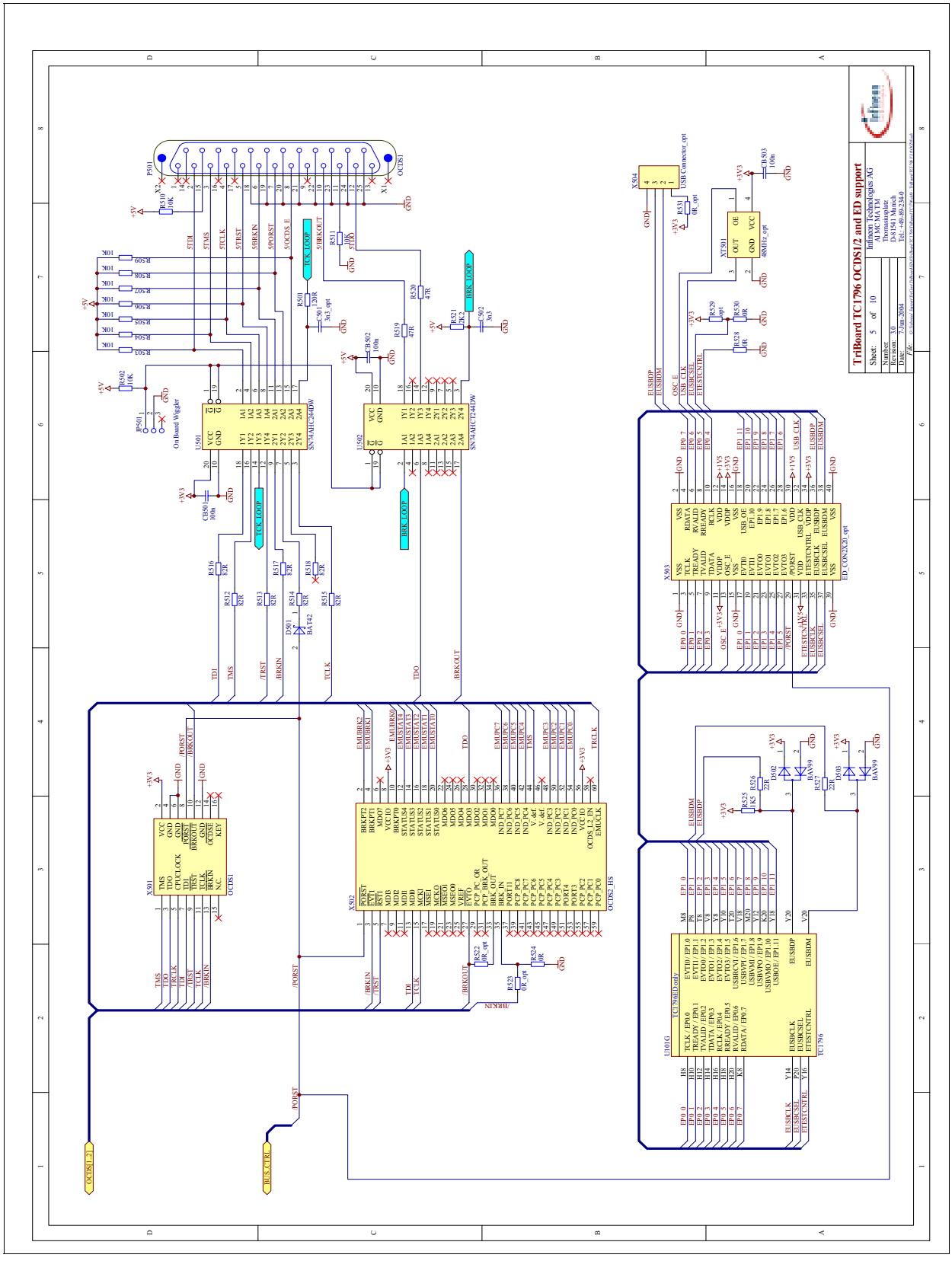

Figure 9-6 Schematic - Debug System

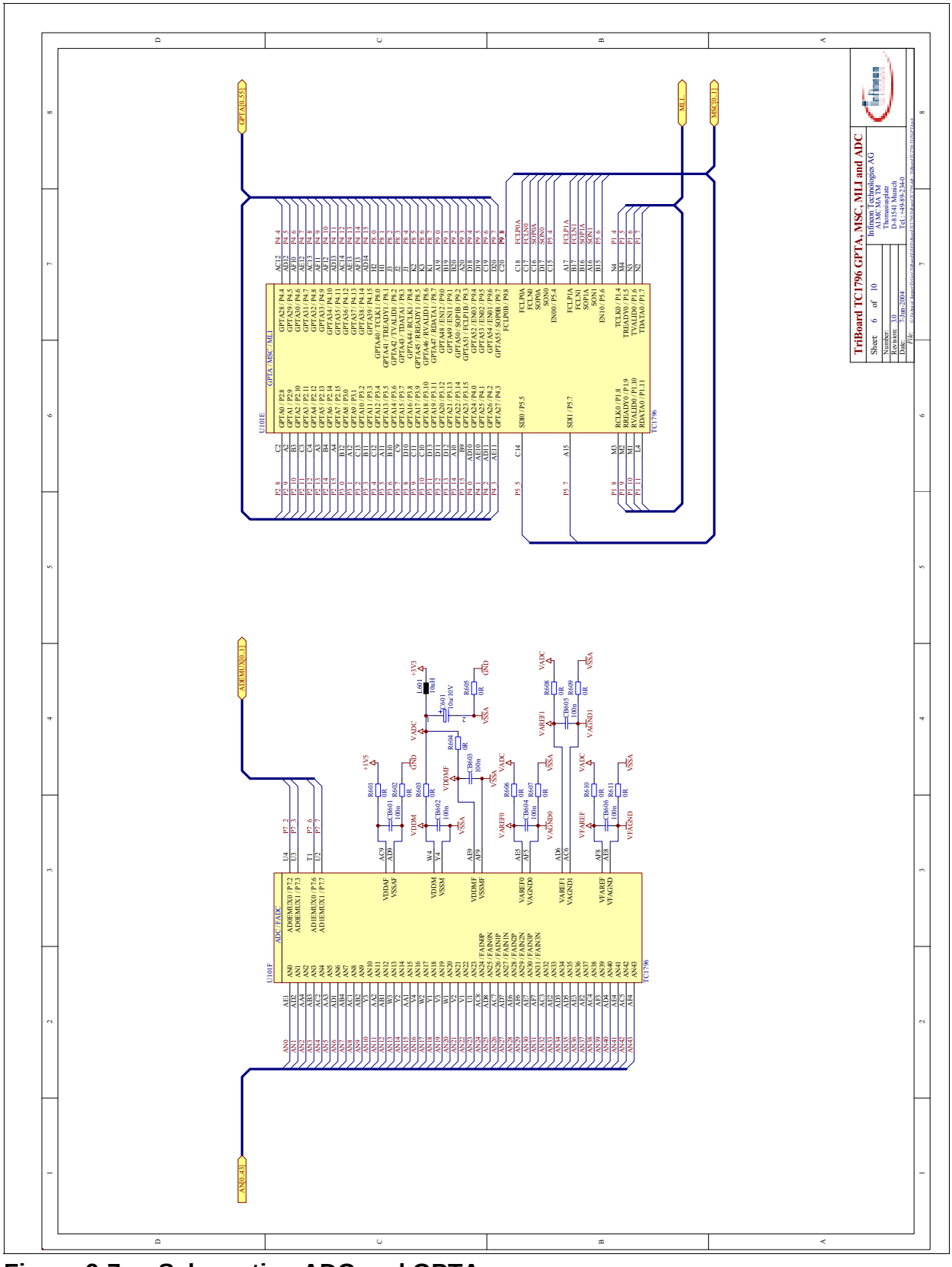

Figure 9-7 Schematic - ADC and GPTA

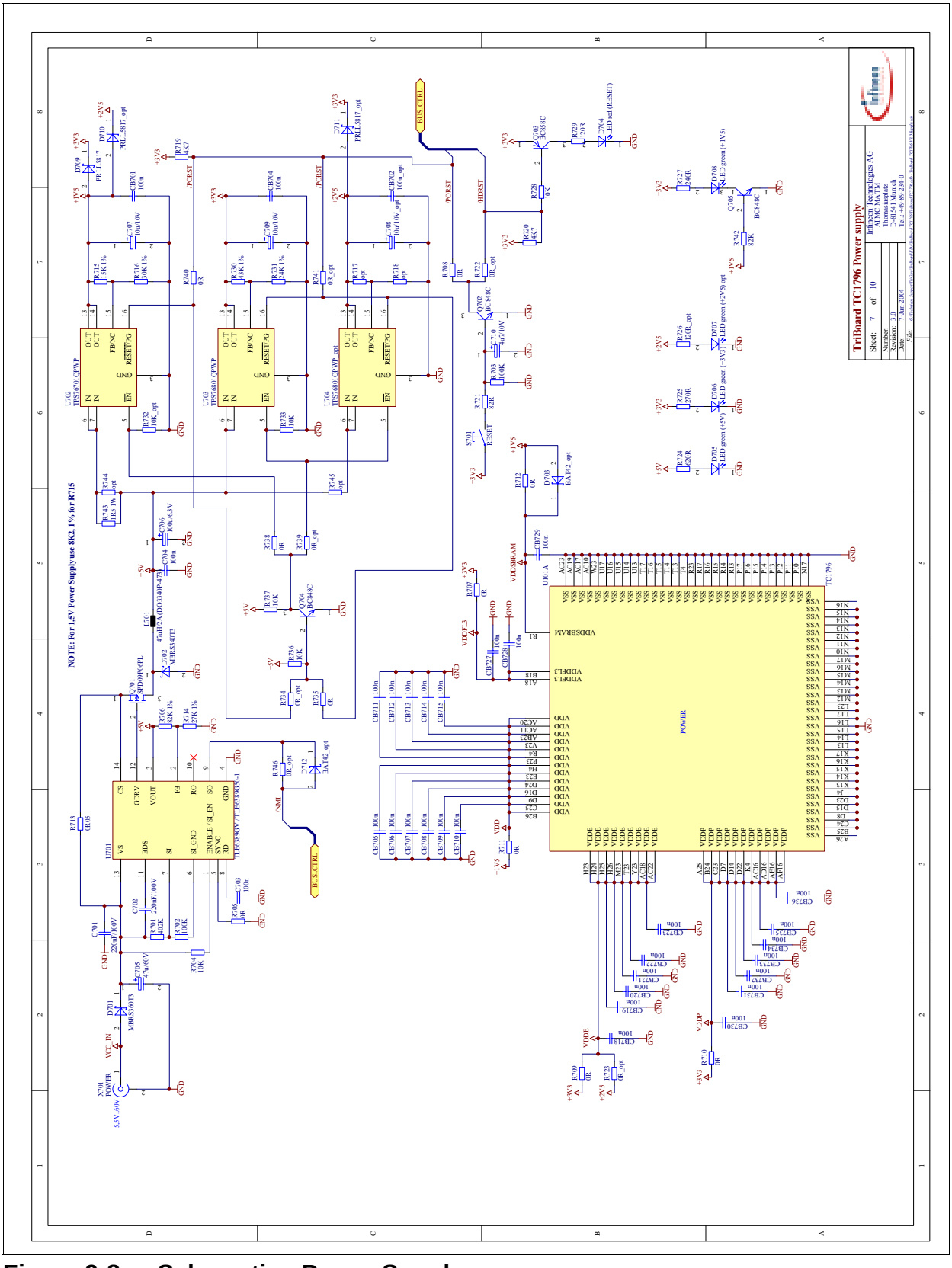

Figure 9-8 Schematic - Power Supply

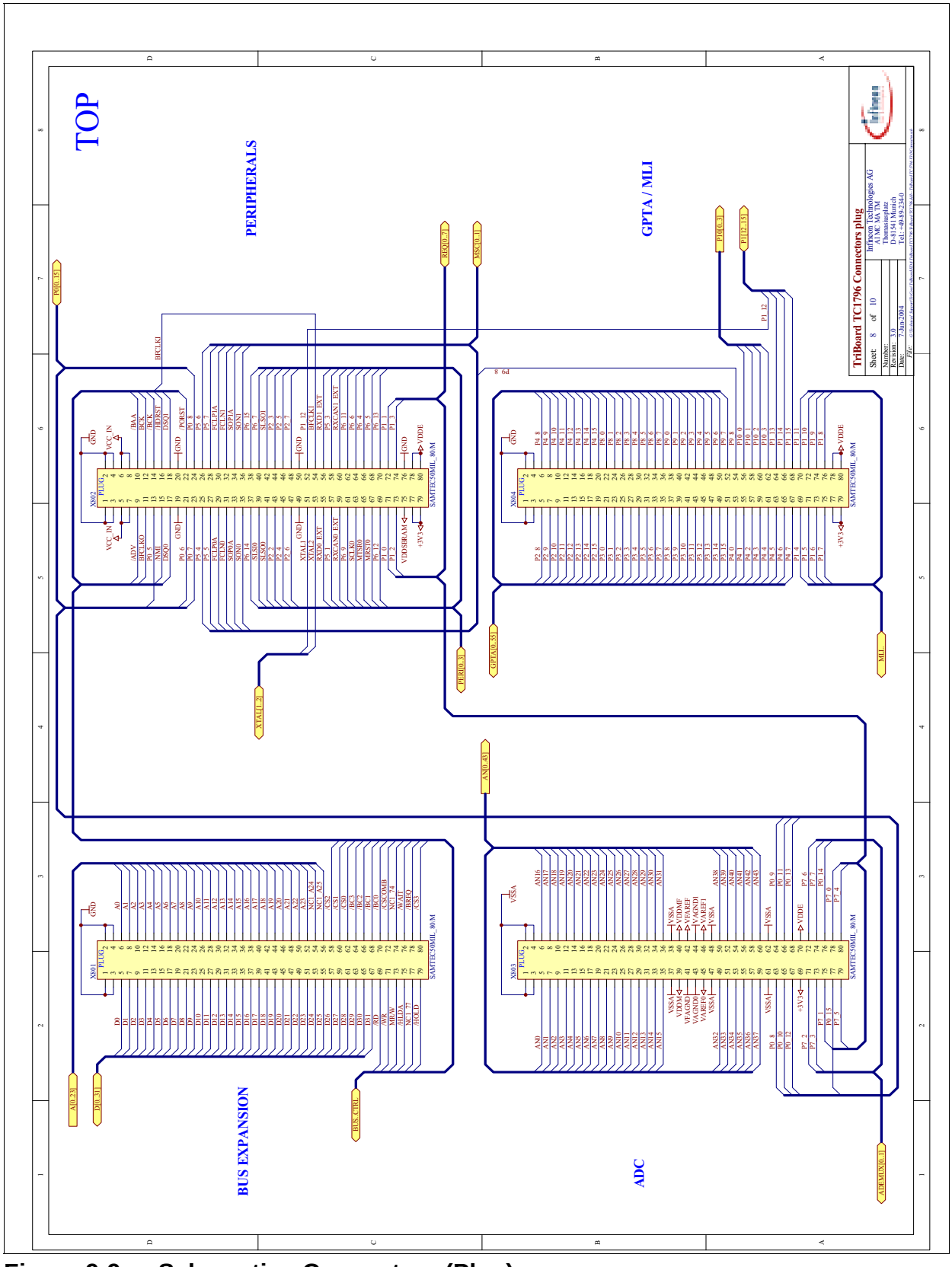

Figure 9-9 Schematic - Connectors (Plug)

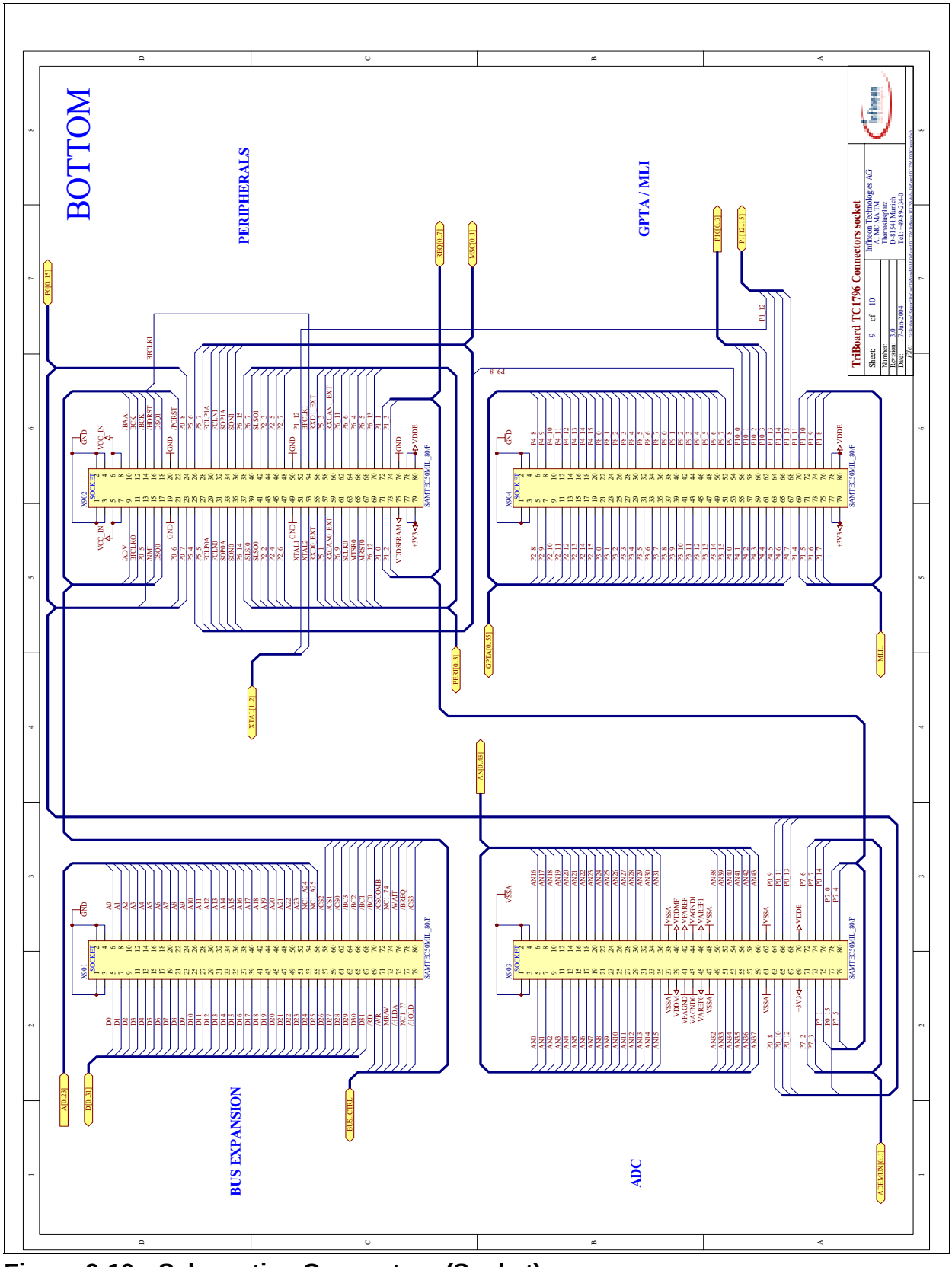

Figure 9-10 Schematic - Connectors (Socket)

9.2 Layout

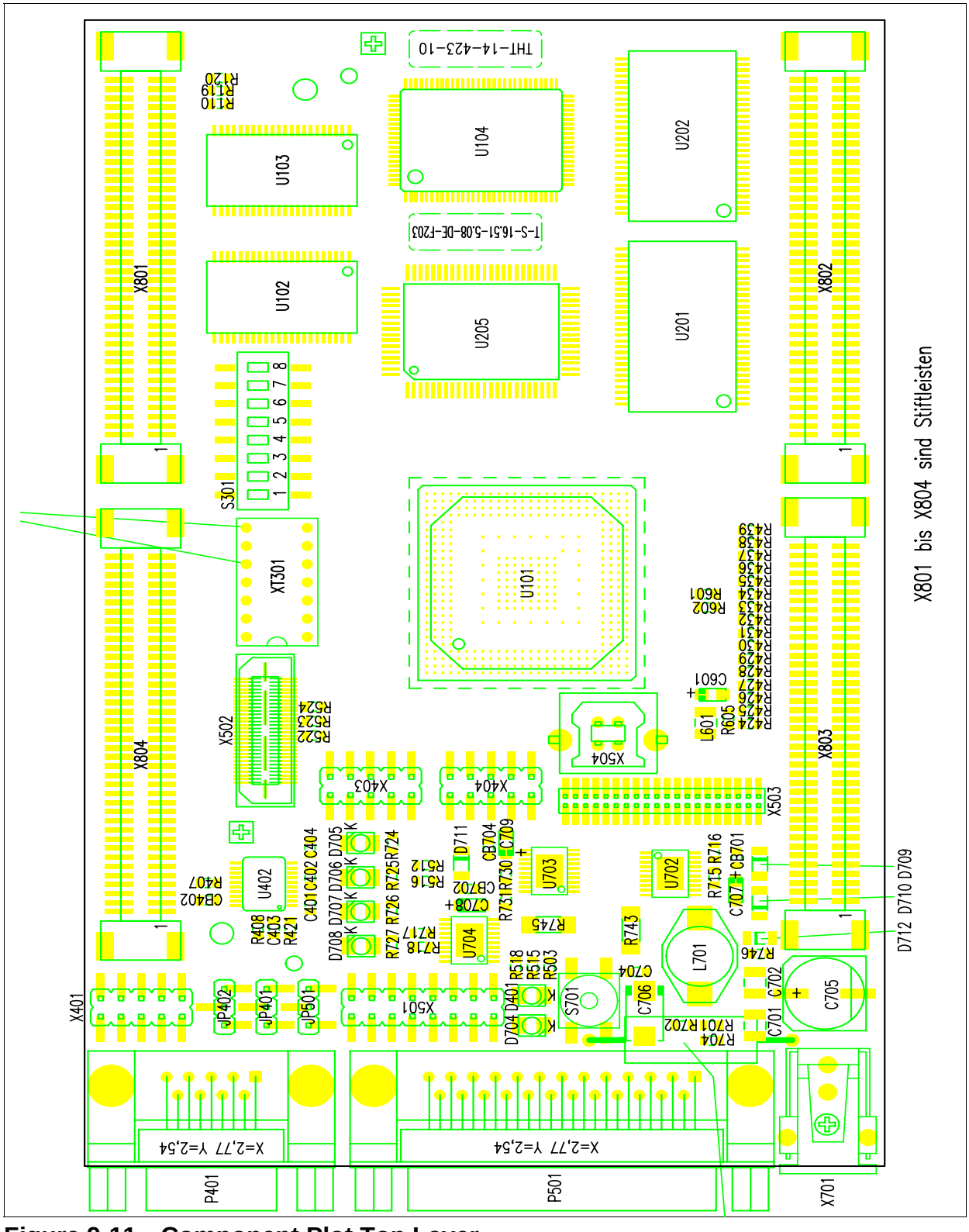

Figure 9-11 Component Plot Top Layer

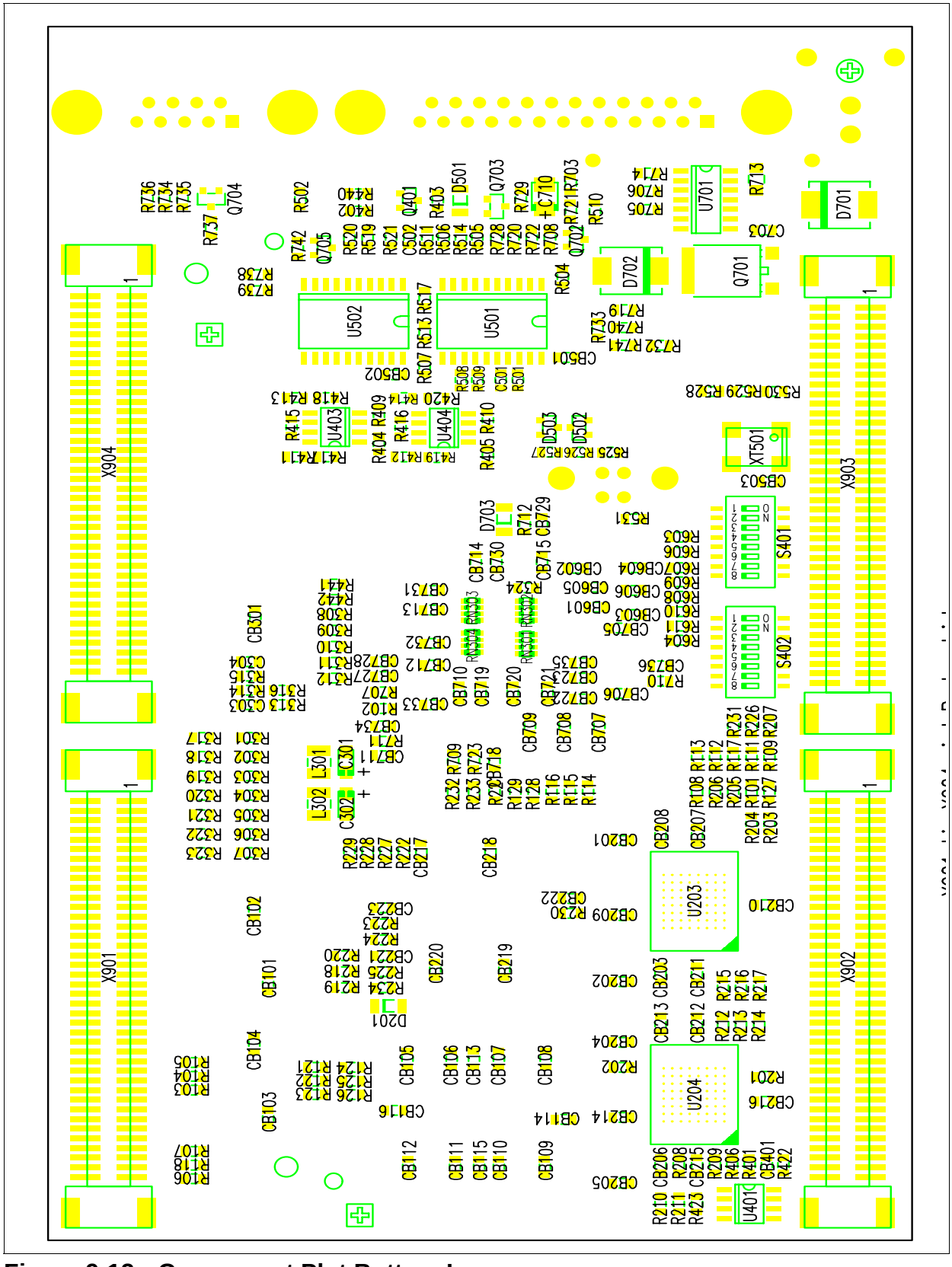

Figure 9-12 Component Plot Bottom Layer

9.3 Layout with Dimensioning

The following dimensions should be used for development of extension boards.

Note: these are the pictures from the TriBoard TC10GP. Connectors X801...X804 are on the same place.

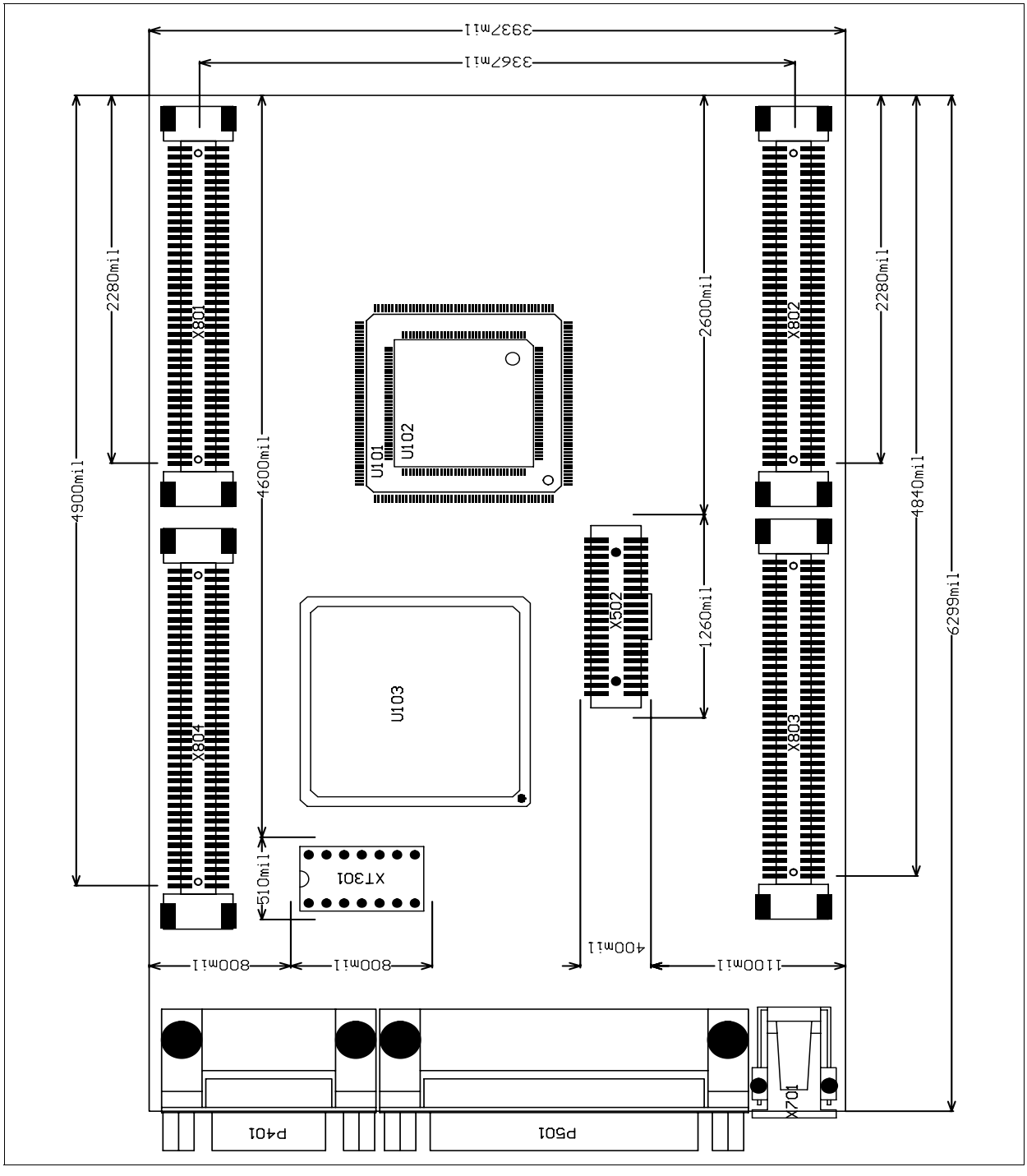

Figure 9-13 Dimensioning (mil)

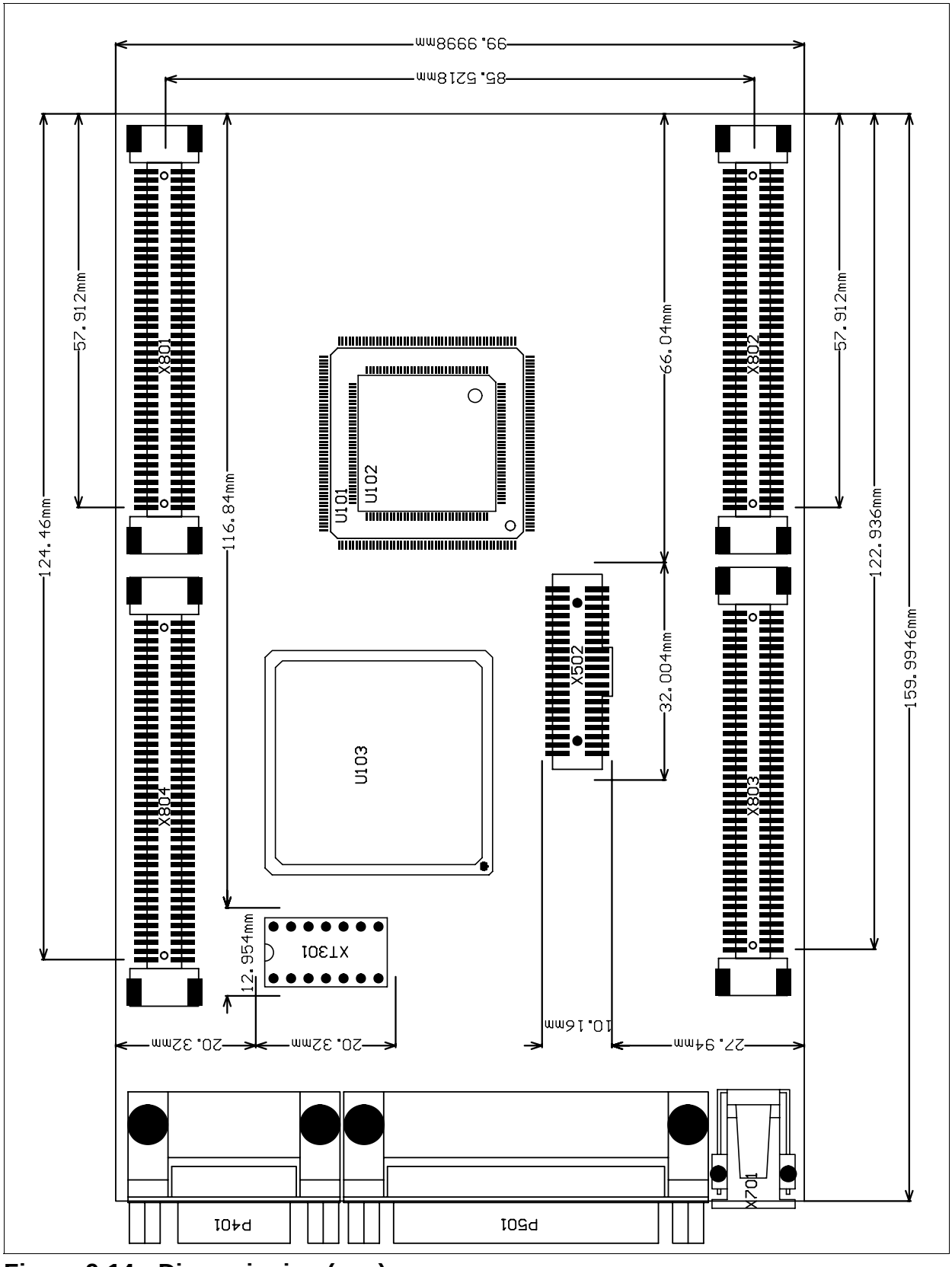

Figure 9-14 Dimensioning (mm)

10 Keyword Index

This section lists a number of keywords which refer to specific details of the TriBoard TC1796 in terms of its architecture, its functional units or functions. This helps to quickly find the answer to specific questions about the TriBoard TC1796.

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4 MBytes Burst Flash (1x32Bit) 4-1
8 MBytes Burst Flash (2x16Bit) 4-1
8 MBytes synchronous SRAM 4-2

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